

MODEL NAME : LA-F371P non-AR
PCB NO : DAA000EC010
BOM P/N : 431A8C31L01

Dell/Compal Confidential

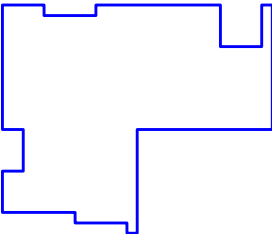
Schematic Document

Pebble Creek MLK (KabyLake R/U)

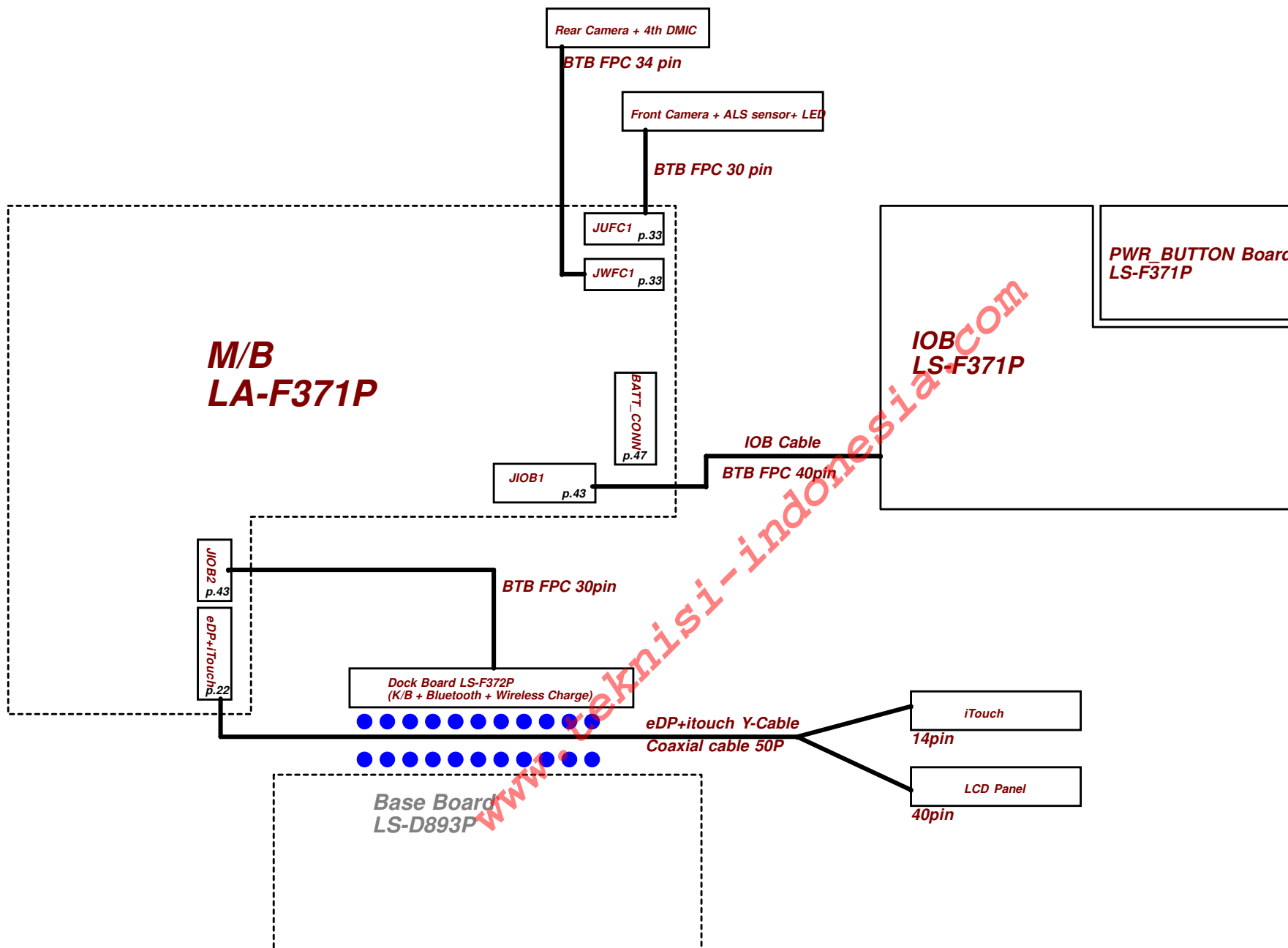
2017-11-03

Rev: 1.0

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				Date: Tuesday, November 07, 2017	Sheet 1 of 65



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				Size	Document Number	Rev
					LA-F371P	1.0
				Date:	Tuesday, November 07, 2017	Sheet 3 of 65

Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	
0	240K +/- 5%	4700p		
1	130K +/- 5%	4700p	Pre-EVT1	
2	62K +/- 5%	4700p	EVT1	
3	33K +/- 5%	4700p	DVT1	
4	8.2K +/- 5%	4700p	DVT2	
5	4.3K +/- 5%	4700p	PVT	
6	2K +/- 5%	4700p		
7	NC			

Board ID Table

Board ID	PCB Revision
0	
1	0.1
2	0.2
3	0.3
4	0.4
5	1.0
6	
7	

USB 3.0

Flexible I/O	Interface	DESTINATION
1	USB 3.0 #1	USB Type-C Port-A
2	USB 3.0 #2/SSIC	NGFF (WWAN)
3	USB 3.0 #3	USB 3.0 Type-A
4	USB 3.0 #4	USB Type-C Port-B
5	PCI-E#1 / USB 3.0#5	Reserved for AR
6	PCI-E#2 / USB 3.0#6	Reserved for AR
7	PCI-E #3	Reserved for AR
8	PCI-E #4	Reserved for AR
9	PCI-E #5	NGFF (WLAN)
10	PCI-E #6	
11	PCI-E #7	NGFF (SSD)
12	PCI-E #8 /SATA #1	NGFF (SSD) #7/#8 2lane PCI-E
13	PCI-E #9	Card Reader
14	PCI-E #10	
15	PCI-E #11	NGFF (WWAN/2nd SSD)
16	PCI-E #12	NGFF (WWAN/2nd SSD)

SMBUS Control Table

	SOURCE	Base	BATT	Charger	XDP	USH	PD Controller	Trinity Dock	P-Sensor	MUX	IMVP	IO Expendor
No use	PCH_SML0CLK PCH_SML0DATA	PCH										
	PCH_SML1CLK PCH_SML1DATA	PCH										
	SMBCLK SMBDATA	PCH			V							
	EC_SMB00_CLK EC_SMB00_DAT	MECS105				V	V			V		
	EC_SMB01_CLK EC_SMB01_DAT	MECS105									V	
	EC_SMB02_CLK EC_SMB02_DAT	MECS105		V								V
	EC_SMB03_CLK EC_SMB03_DAT	MECS105										
	EC_SMB04_CLK EC_SMB04_DAT	MECS105					V		V	V		
	EC_SMB05_CLK EC_SMB05_DAT	MECS105	V					V				
	EC_SMB10_CLK EC_SMB10_DAT	MECS105		V								

Link

Port Mapping USB 2.0 CLK

USB 2.0 PORT#	DESTINATION
1	Type-C Port-A
2	Dock
3	Type-C Port-B
4	WWAN
5	IR CAM
7	WLAN
9	USB Type-A
10	USH

	DIFFERENTIAL	DESTINATION
CLK	CLKOUT_PCIE0	
	CLKOUT_PCIE1	NGFF (WLAN)
	CLKOUT_PCIE2	NGFF (WWAN)
	CLKOUT_PCIE3	SSD
	CLKOUT_PCIE5	Card Reader
	FLEX CLOCKS	DESTINATION
	CLKOUT_LPC_0	ESPI
	CLKOUT_LPC_1	ESPI

Displayport

	DDI PORT#	DESTINATION
DDI	1	USB Type-C Port-B
	2	USB Type-C Port-A

Symbol Note :

@ : means de-pop

⏏ : means Digital Ground

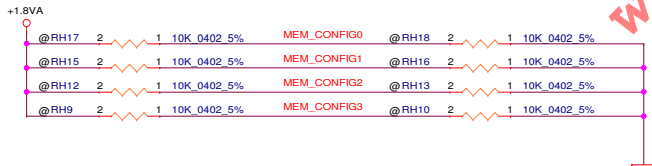
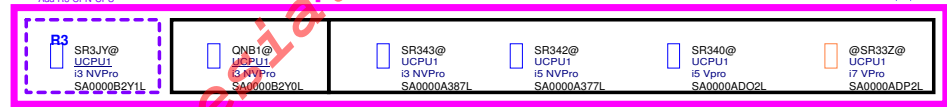
⏏ : means Analog Ground









































Type-C PortA



4+2 CPU Option

2+2 CPU Option



X76		DRAM Option (R1) , R3 check P08				DRAM Config Option (Resistor pop location)			
		MEM_CONFIG0				MEM_CONFIG1	MEM_CONFIG2	MEM_CONFIG3	
X7669231L05		Micron 8G/1866  MICRON_8G@UD1 MT52L256M32D1PF-107WT SA00009XUOL				 MICRON_8G@UD2 MT52L256M32D1PF-107WT SA00009XUOL	 MICRON_8G@UD3 MT52L256M32D1PF-107WT SA00009XUOL	 MICRON_8G@UD4 MT52L256M32D1PF-107WT SA00009XUOL	
X7669231L07		Micron 16G/1866  MICRON_16G@UD1 MT52L512M32D2PF-107WT SA00009U7OL				 MICRON_16G@UD2 MT52L512M32D2PF-107WT SA00009U7OL	 MICRON_16G@UD3 MT52L512M32D2PF-107WT SA00009U7OL	 MICRON_16G@UD4 MT52L512M32D2PF-107WT SA00009U7OL	
X7669231L09		Micron 32G/1866  MICRON_32G@UD1 MT52L1G32D4PG-107WT SA00009XVOL				 MICRON_32G@UD2 MT52L1G32D4PG-107WT SA00009XVOL	 MICRON_32G@UD3 MT52L1G32D4PG-107WT SA00009XVOL	 MICRON_32G@UD4 MT52L1G32D4PG-107WT SA00009XVOL	
X7669231L06		Hynix 8G/1866  HYNIX_8G@UD1 H9CCNNN83TMLAR-NUD FBG SA00008G64L				 HYNIX_8G@UD2 H9CCNNN83TMLAR-NUD FBG SA00008G64L	 HYNIX_8G@UD3 H9CCNNN83TMLAR-NUD FBG SA00008G64L	 HYNIX_8G@UD4 H9CCNNN83TMLAR-NUD FBG SA00008G64L	
X7669231L08		Hynix 16G/1866  HYNIX_16G@UD1 H9CCNNNB1TMLAR-NUD FBG SA00008FJ4L				 HYNIX_16G@UD2 H9CCNNNB1TMLAR-NUD FBG SA00008FJ4L	 HYNIX_16G@UD3 H9CCNNNB1TMLAR-NUD FBG SA00008FJ4L	 HYNIX_16G@UD4 H9CCNNNB1TMLAR-NUD FBG SA00008FJ4L	
X7669231L10		Hynix 32G/1866  HYNIX_32G@UD1 H9CCNNNCLTMLAR-NUD FBG SA0000AFNOL				 HYNIX_32G@UD2 H9CCNNNCLTMLAR-NUD FBG SA0000AFNOL	 HYNIX_32G@UD3 H9CCNNNCLTMLAR-NUD FBG SA0000AFNOL	 HYNIX_32G@UD4 H9CCNNNCLTMLAR-NUD FBG SA0000AFNOL	
X7669231L01		Samsung 8G/1866  SAMSUNG_8G@UD1 K4E6E304EB-EGCF FBGA178 SA00009XYOL				 SAMSUNG_8G@UD2 K4E6E304EB-EGCF FBGA178 SA00009XYOL	 SAMSUNG_8G@UD3 K4E6E304EB-EGCF FBGA178 SA00009XYOL	 SAMSUNG_8G@UD4 K4E6E304EB-EGCF FBGA178 SA00009XYOL	
X7669231L02		Samsung 16G/1866  SAMSUNG_16G@UD1 K4E6E304EB-EGCF FBGA17 SA00008QV2L				 SAMSUNG_16G@UD2 K4E6E304EB-EGCF FBGA17 SA00008QV2L	 SAMSUNG_16G@UD3 K4E6E304EB-EGCF FBGA17 SA00008QV2L	 SAMSUNG_16G@UD4 K4E6E304EB-EGCF FBGA17 SA00008QV2L	
X7669231L03		Samsung 32G/1866  SAMSUNG_32G@UD1 SAMSUNG_32G@UD2 SA00008QV2L				 SAMSUNG_32G@UD2 SAMSUNG_32G@UD3 SA00008QV2L	 SAMSUNG_32G@UD3 SAMSUNG_32G@UD4 SA00008QV2L	 SAMSUNG_32G@UD4 SAMSUNG_32G@RH9 SA00008QV2L	
X7669231L03		Samsung 32G/1866  SAMSUNG_32G@UD1 SAMSUNG_32G@UD2 SA00008QV2L				 SAMSUNG_32G@UD2 SAMSUNG_32G@UD3 SA00008QV2L	 SAMSUNG_32G@UD3 SAMSUNG_32G@UD4 SA00008QV2L	 SAMSUNG_32G@UD4 SAMSUNG_32G@RH9 SA00008QV2L	

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				LA-F371P		
				Date:	Tuesday, November 07, 2017	Sheet 5 of 65

LPDDR3, Ballout for side by side(Non-Interleave)

19	DDR_A_DQS[0..7]	20	DDR_B_DQS[0..7]
19	DDR_A_DQS[0..7]	20	DDR_B_DQS[0..7]
19	DDR_A_D[0..63]	20	DDR_B_D[0..63]
19,21	DDR_A_CA1[0..9]	20,21	DDR_B_CA1[0..9]
19,21	DDR_A_CA2[0..9]	20,21	DDR_B_CA2[0..9]

@UCPU1B

SKL-U

DDR_A_D0 AL71	DDR0_DQ[0]	DDR0_CK[0]	AU53	DDR_A_CLK#0	DDR_A_CLK#0	19,21
DDR_A_D1 AL68	DDR0_DQ[1]	DDR0_CK[1]	AT53	DDR_A_CLK#1	DDR_A_CLK#1	19,21
DDR_A_D2 AN68	DDR0_DQ[2]	DDR0_CK[1]	AT55	DDR_A_CLK#1	DDR_A_CLK#1	19,21
DDR_A_D3 AN69	DDR0_DQ[3]	DDR0_CK[1]				
DDR_A_D4 AL70	DDR0_DQ[4]		BA56	DDR_A_CKE0	DDR_A_CKE0	19,21
DDR_A_D5 AL69	DDR0_DQ[5]	DDR0_CKE[0]	BA56	DDR_A_CKE1	DDR_A_CKE1	19,21
DDR_A_D6 AN70	DDR0_DQ[6]	DDR0_CKE[1]	AW56	DDR_A_CKE2	DDR_A_CKE2	19,21
DDR_A_D7 AN71	DDR0_DQ[7]	DDR0_CKE[2]	AY56	DDR_A_CKE3	DDR_A_CKE3	19,21
DDR_A_D8 AR70	DDR0_DQ[8]	DDR0_CKE[3]				
DDR_A_D9 AR68	DDR0_DQ[9]		AU46	DDR_A_CS#0	DDR_A_CS#0	19,21
DDR_A_D10 AU71	DDR0_DQ[10]	DDR0_CS[0]	AU43	DDR_A_CS#1	DDR_A_CS#1	19,21
DDR_A_D11 AU68	DDR0_DQ[11]	DDR0_CS[1]	AT45	DDR_A_ODT0	DDR_A_ODT0	19,21
DDR_A_D12 AR71	DDR0_DQ[12]	DDR0_ODT[0]	AT43			
DDR_A_D13 AR69	DDR0_DQ[13]	DDR0_ODT[1]				
DDR_A_D14 AU70	DDR0_DQ[14]		BA51	DDR_A_CA1_0	DDR_A_CA1_0	19,21
DDR_A_D15 AU69	DDR0_DQ[15]	DDR0_MA[5]DDR0_CAA[0]DDR0_MA[5]	BB54	DDR_A_CA1_1	DDR_A_CA1_1	19,21
DDR_A_D16 BB65	DDR0_DQ[16]DDR0_DQ[32]	DDR0_MA[6]DDR0_CAA[1]DDR0_MA[6]	BA52	DDR_A_CA1_2	DDR_A_CA1_2	19,21
DDR_A_D17 BB65	DDR0_DQ[17]DDR0_DQ[33]	DDR0_MA[7]DDR0_CAA[2]DDR0_MA[7]	AY52	DDR_A_CA1_3	DDR_A_CA1_3	19,21
DDR_A_D18 BB65	DDR0_DQ[18]DDR0_DQ[34]	DDR0_MA[8]DDR0_CAA[3]DDR0_MA[8]	AW52	DDR_A_CA1_4	DDR_A_CA1_4	19,21
DDR_A_D19 BB65	DDR0_DQ[19]DDR0_DQ[35]	DDR0_MA[9]DDR0_CAA[4]DDR0_MA[9]	AY55	DDR_A_CA1_5	DDR_A_CA1_5	19,21
DDR_A_D20 BB65	DDR0_DQ[20]DDR0_DQ[36]	DDR0_MA[10]DDR0_CAA[5]DDR0_MA[10]	AW54	DDR_A_CA1_6	DDR_A_CA1_6	19,21
DDR_A_D21 BB65	DDR0_DQ[21]DDR0_DQ[37]	DDR0_MA[11]DDR0_CAA[6]DDR0_MA[11]	BA54	DDR_A_CA1_7	DDR_A_CA1_7	19,21
DDR_A_D22 BB63	DDR0_DQ[22]DDR0_DQ[38]	DDR0_MA[12]DDR0_CAA[7]DDR0_MA[12]	BA55	DDR_A_CA1_8	DDR_A_CA1_8	19,21
DDR_A_D23 BB63	DDR0_DQ[23]DDR0_DQ[39]	DDR0_MA[13]DDR0_CAA[8]DDR0_MA[13]	AY54	DDR_A_CA1_9	DDR_A_CA1_9	19,21
DDR_A_D24 BB61	DDR0_DQ[24]DDR0_DQ[40]	DDR0_MA[14]DDR0_CAA[9]DDR0_MA[14]				
DDR_A_D25 BB61	DDR0_DQ[25]DDR0_DQ[41]		AU46	DDR_A_CA2_0	DDR_A_CA2_0	19,21
DDR_A_D26 BB59	DDR0_DQ[26]DDR0_DQ[42]	DDR0_MA[15]DDR0_CAB[0]DDR0_MA[15]	AU48	DDR_A_CA2_1	DDR_A_CA2_1	19,21
DDR_A_D27 BB61	DDR0_DQ[27]DDR0_DQ[43]	DDR0_MA[16]DDR0_CAB[1]DDR0_MA[16]	AT46	DDR_A_CA2_2	DDR_A_CA2_2	19,21
DDR_A_D28 BB61	DDR0_DQ[28]DDR0_DQ[44]	DDR0_MA[17]DDR0_CAB[2]DDR0_MA[17]	AU50	DDR_A_CA2_3	DDR_A_CA2_3	19,21
DDR_A_D29 BB61	DDR0_DQ[29]DDR0_DQ[45]	DDR0_MA[18]DDR0_CAB[3]DDR0_MA[18]	AU52	DDR_A_CA2_4	DDR_A_CA2_4	19,21
DDR_A_D30 BB59	DDR0_DQ[30]DDR0_DQ[46]	DDR0_MA[19]DDR0_CAB[4]DDR0_MA[19]	AY51	DDR_A_CA2_5	DDR_A_CA2_5	19,21
DDR_A_D31 BB59	DDR0_DQ[31]DDR0_DQ[47]	DDR0_MA[20]DDR0_CAB[5]DDR0_MA[20]	AT48	DDR_A_CA2_6	DDR_A_CA2_6	19,21
DDR_A_D32 BB59	DDR0_DQ[32]DDR0_DQ[48]	DDR0_MA[21]DDR0_CAB[6]DDR0_MA[21]	AY50	DDR_A_CA2_7	DDR_A_CA2_7	19,21
DDR_A_D33 BB59	DDR0_DQ[33]DDR0_DQ[49]	DDR0_MA[22]DDR0_CAB[7]DDR0_MA[22]	BB50	DDR_A_CA2_8	DDR_A_CA2_8	19,21
DDR_A_D34 BB59	DDR0_DQ[34]DDR0_DQ[50]	DDR0_MA[23]DDR0_CAB[8]DDR0_MA[23]	AU50	DDR_A_CA2_9	DDR_A_CA2_9	19,21
DDR_A_D35 BB59	DDR0_DQ[35]DDR0_DQ[51]	DDR0_MA[24]DDR0_CAB[9]DDR0_MA[24]	BA50			
DDR_A_D36 BB59	DDR0_DQ[36]DDR0_DQ[52]		BB52			
DDR_A_D37 BB59	DDR0_DQ[37]DDR0_DQ[53]	DDR0_MA[25]DDR0_CAB[10]DDR0_MA[25]	AM70	DDR_A_DQS#0	DDR_A_DQS#0	19
DDR_A_D38 BB59	DDR0_DQ[38]DDR0_DQ[54]	DDR0_MA[26]DDR0_CAB[11]DDR0_MA[26]	AM69	DDR_A_DQS#1	DDR_A_DQS#1	19
DDR_A_D39 BB59	DDR0_DQ[39]DDR0_DQ[55]	DDR0_MA[27]DDR0_CAB[12]DDR0_MA[27]	AT69	DDR_A_DQS#2	DDR_A_DQS#2	19
DDR_A_D40 BB59	DDR0_DQ[40]DDR0_DQ[56]	DDR0_MA[28]DDR0_CAB[13]DDR0_MA[28]	AT70	DDR_A_DQS#3	DDR_A_DQS#3	19
DDR_A_D41 BB59	DDR0_DQ[41]DDR0_DQ[57]	DDR0_MA[29]DDR0_CAB[14]DDR0_MA[29]	BA64	DDR_A_DQS#4	DDR_A_DQS#4	19
DDR_A_D42 BB59	DDR0_DQ[42]DDR0_DQ[58]	DDR0_MA[30]DDR0_CAB[15]DDR0_MA[30]	AY64	DDR_A_DQS#5	DDR_A_DQS#5	19
DDR_A_D43 BB59	DDR0_DQ[43]DDR0_DQ[59]	DDR0_MA[31]DDR0_CAB[16]DDR0_MA[31]	AY60	DDR_A_DQS#6	DDR_A_DQS#6	19
DDR_A_D44 BB59	DDR0_DQ[44]DDR0_DQ[60]	DDR0_MA[32]DDR0_CAB[17]DDR0_MA[32]	BA60	DDR_A_DQS#7	DDR_A_DQS#7	19
DDR_A_D45 BB59	DDR0_DQ[45]DDR0_DQ[61]	DDR0_MA[33]DDR0_CAB[18]DDR0_MA[33]	BA38	DDR_A_DQS#8	DDR_A_DQS#8	19
DDR_A_D46 BB59	DDR0_DQ[46]DDR0_DQ[62]	DDR0_MA[34]DDR0_CAB[19]DDR0_MA[34]	AY38	DDR_A_DQS#9	DDR_A_DQS#9	19
DDR_A_D47 BB59	DDR0_DQ[47]DDR0_DQ[63]	DDR0_MA[35]DDR0_CAB[20]DDR0_MA[35]	AY34	DDR_A_DQS#10	DDR_A_DQS#10	19
DDR_A_D48 BB59	DDR0_DQ[48]DDR0_DQ[64]	DDR0_MA[36]DDR0_CAB[21]DDR0_MA[36]	BA34	DDR_A_DQS#11	DDR_A_DQS#11	19
DDR_A_D49 BB59	DDR0_DQ[49]DDR0_DQ[65]	DDR0_MA[37]DDR0_CAB[22]DDR0_MA[37]	BA30	DDR_A_DQS#12	DDR_A_DQS#12	19
DDR_A_D50 BB59	DDR0_DQ[50]DDR0_DQ[66]	DDR0_MA[38]DDR0_CAB[23]DDR0_MA[38]	AY30	DDR_A_DQS#13	DDR_A_DQS#13	19
DDR_A_D51 BB59	DDR0_DQ[51]DDR0_DQ[67]	DDR0_MA[39]DDR0_CAB[24]DDR0_MA[39]	AY26	DDR_A_DQS#14	DDR_A_DQS#14	19
DDR_A_D52 BB59	DDR0_DQ[52]DDR0_DQ[68]	DDR0_MA[40]DDR0_CAB[25]DDR0_MA[40]	BA26	DDR_A_DQS#15	DDR_A_DQS#15	19
DDR_A_D53 BB59	DDR0_DQ[53]DDR0_DQ[69]	DDR0_MA[41]DDR0_CAB[26]DDR0_MA[41]				
DDR_A_D54 BB59	DDR0_DQ[54]DDR0_DQ[70]	DDR0_MA[42]DDR0_CAB[27]DDR0_MA[42]	AW50	DDR_A_ALERT#	DDR_A_ALERT#	19
DDR_A_D55 BB59	DDR0_DQ[55]DDR0_DQ[71]	DDR0_MA[43]DDR0_CAB[28]DDR0_MA[43]	AT52	DDR_A_VREF#	DDR_A_VREF#	19
DDR_A_D56 BB59	DDR0_DQ[56]DDR0_DQ[72]	DDR0_MA[44]DDR0_CAB[29]DDR0_MA[44]	AY67	DDR_A_VREF#	DDR_A_VREF#	19
DDR_A_D57 BB59	DDR0_DQ[57]DDR0_DQ[73]	DDR0_MA[45]DDR0_CAB[30]DDR0_MA[45]	AY68	DDR_A_VREF#	DDR_A_VREF#	19
DDR_A_D58 BB59	DDR0_DQ[58]DDR0_DQ[74]	DDR0_MA[46]DDR0_CAB[31]DDR0_MA[46]	BA67	DDR_A_VREF#	DDR_A_VREF#	19
DDR_A_D59 BB59	DDR0_DQ[59]DDR0_DQ[75]	DDR0_MA[47]DDR0_CAB[32]DDR0_MA[47]				
DDR_A_D60 BB59	DDR0_DQ[60]DDR0_DQ[76]	DDR0_MA[48]DDR0_CAB[33]DDR0_MA[48]				
DDR_A_D61 BB59	DDR0_DQ[61]DDR0_DQ[77]	DDR0_MA[49]DDR0_CAB[34]DDR0_MA[49]				
DDR_A_D62 BB59	DDR0_DQ[62]DDR0_DQ[78]	DDR0_MA[50]DDR0_CAB[35]DDR0_MA[50]				
DDR_A_D63 BB59	DDR0_DQ[63]DDR0_DQ[79]	DDR0_MA[51]DDR0_CAB[36]DDR0_MA[51]				

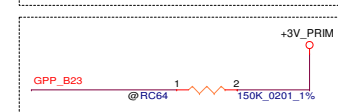
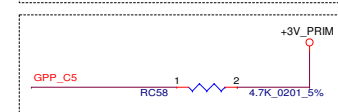
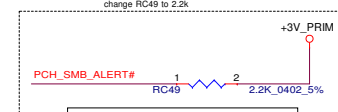
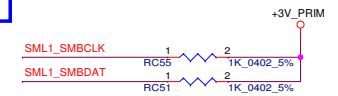
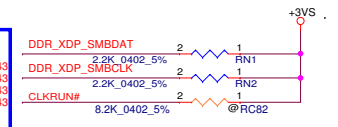
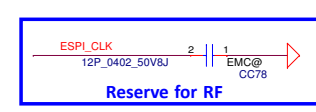
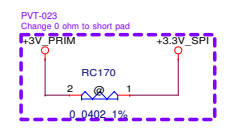
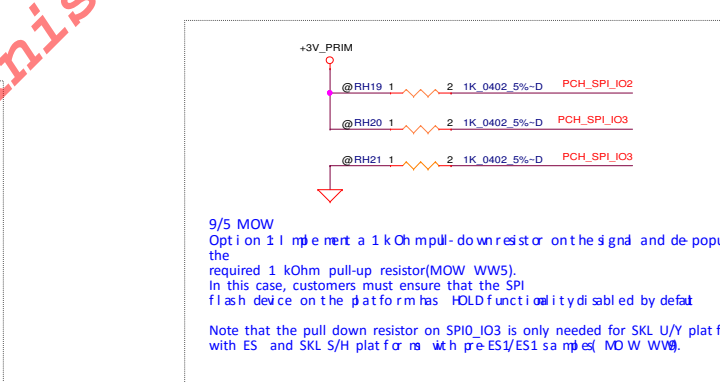
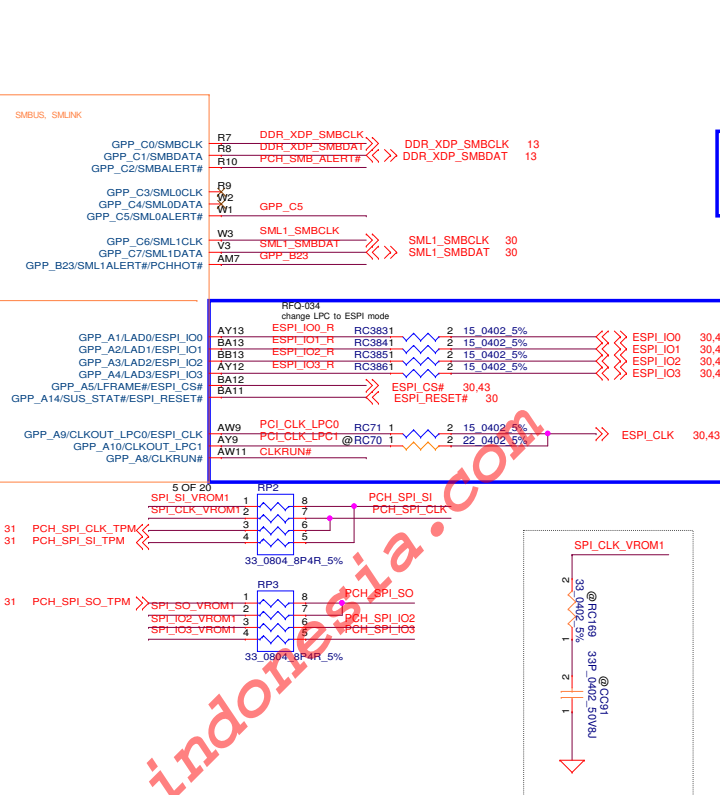
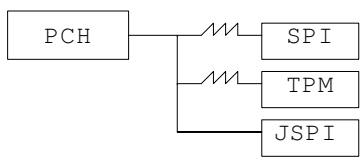
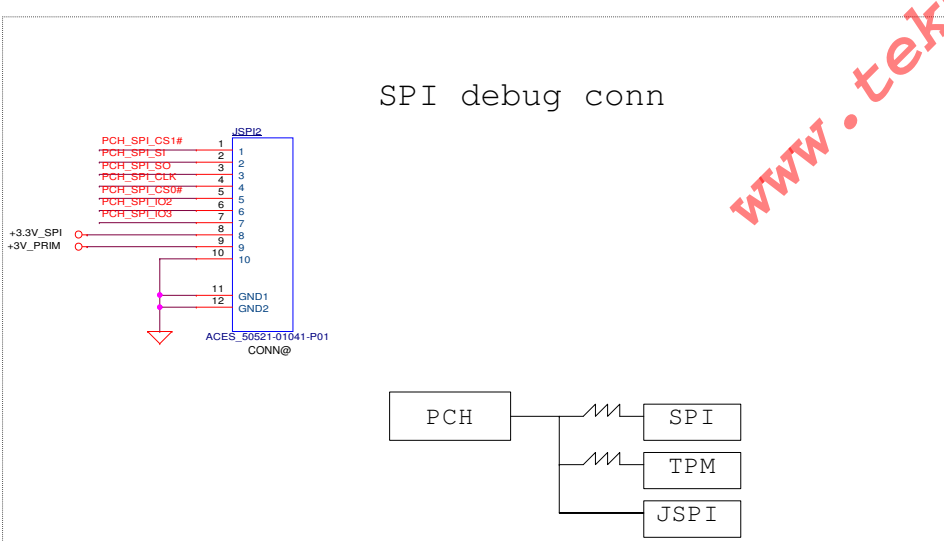
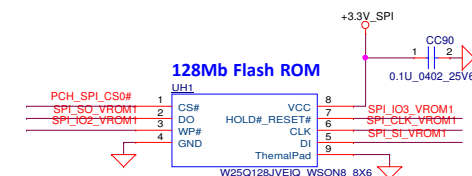
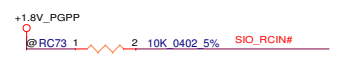
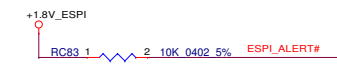
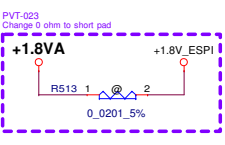
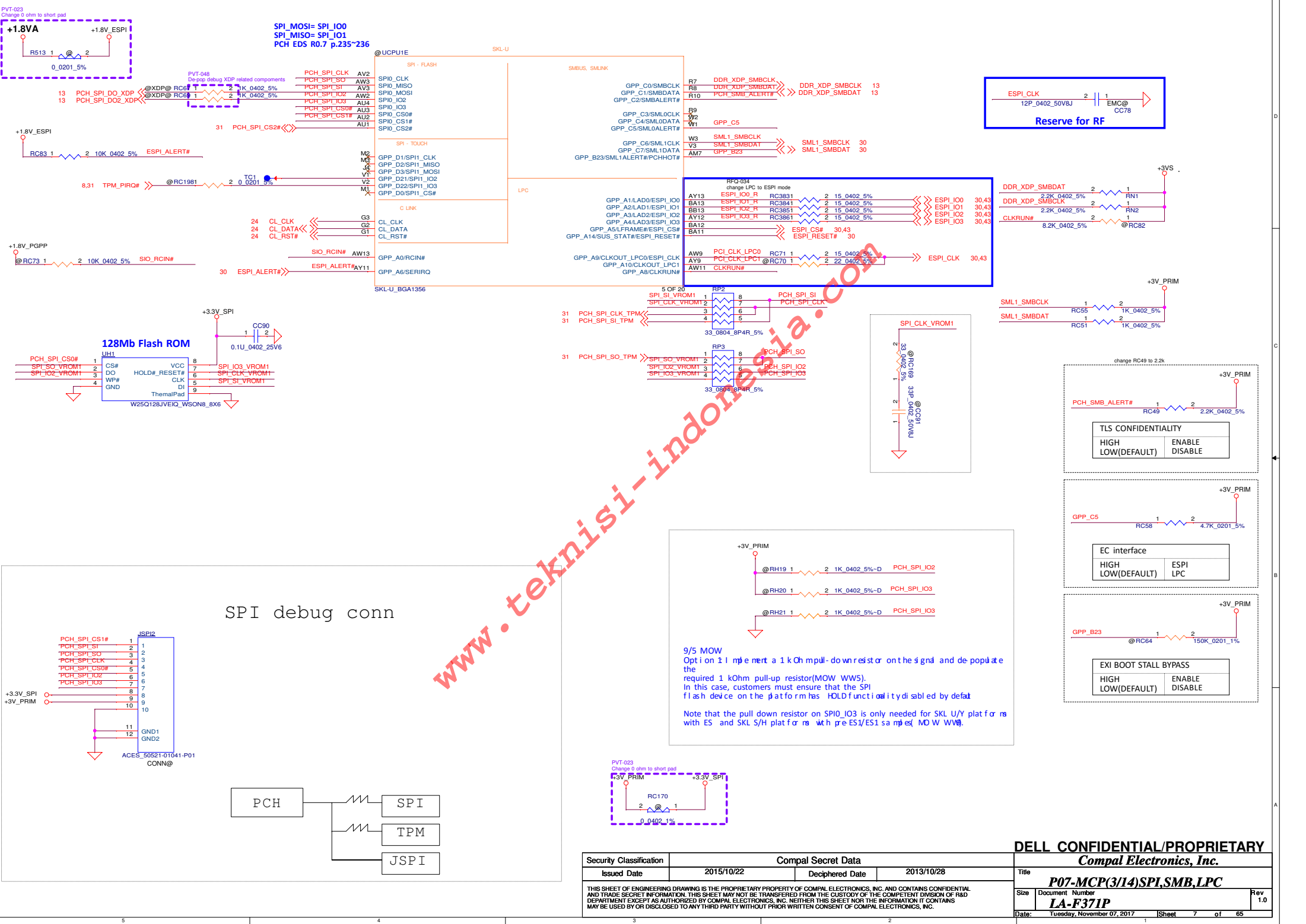
SKL-U_BGA1356

2 OF 20

@UCPU1C

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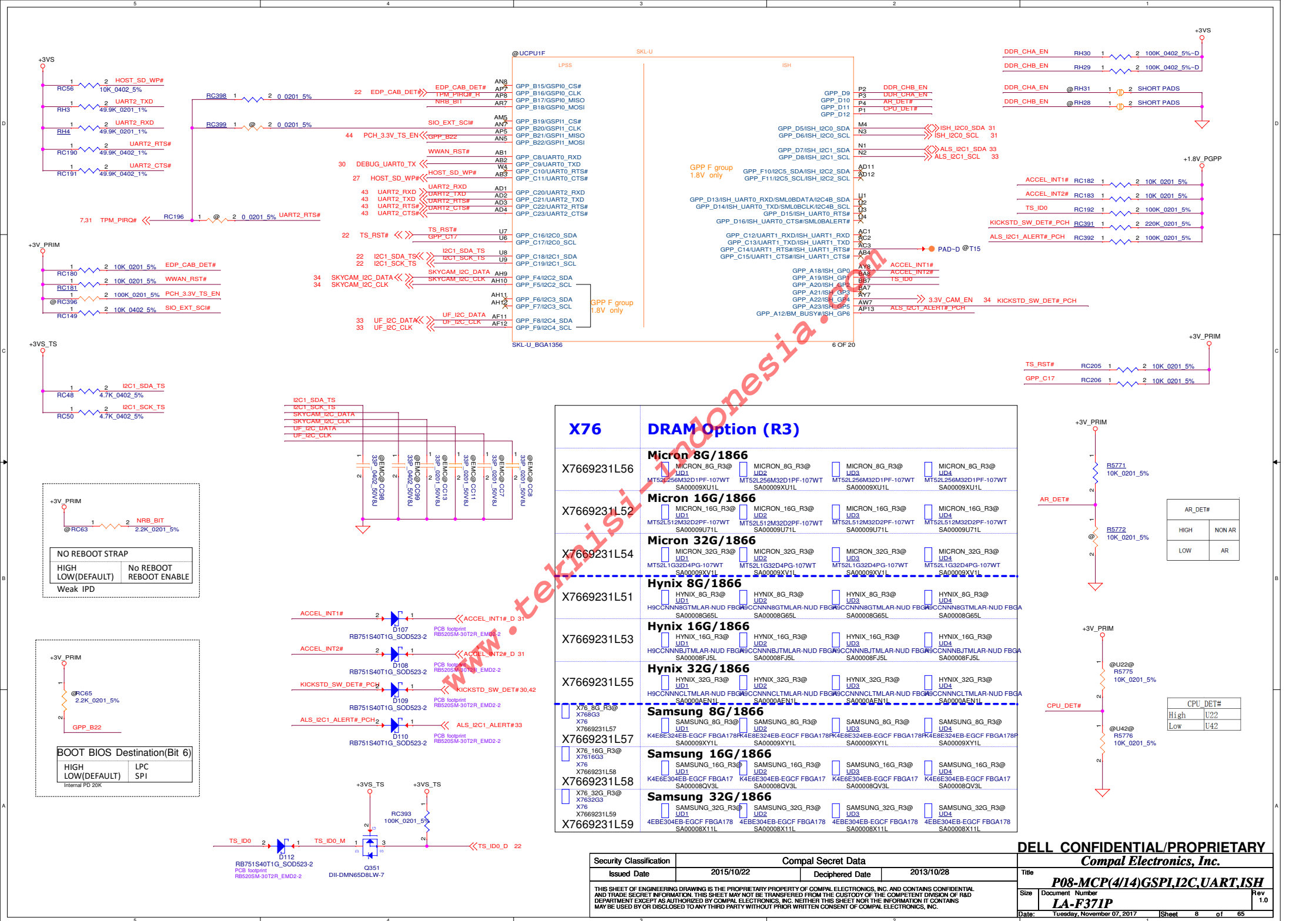
DDR_A_D16	AF65	DDR1_DQ[0]DDR0_DQ[16]	DDR1_CK[0]	AN46	DDR_B_CLK#0	DDR_B_CLK#0	20,21
DDR_A_D17	AF64	DDR1_DQ[1]DDR0_DQ[17]	DDR1_CK[1]	AN46	DDR_B_CLK#0	DDR_B_CLK#0	20,21
DDR_A_D18	AK65	DDR1_DQ[2]DDR0_DQ[18]	DDR1_CK[1]	AP45	DDR_B_CLK#0	DDR_B_CLK#0	20,21
DDR_A_D19	AK64	DDR1_DQ[3]DDR0_DQ[19]	DDR1_CK[1]	AP46	DDR_B_CLK#1	DDR_B_CLK#1	20,21
DDR_A_D20	AF66	DDR1_DQ[4]DDR0_DQ[20]	DDR1_CK[1]			DDR_B_CLK0	20,21
DDR_A_D21	AF67	DDR1_DQ[4]DDR0_DQ[20]	DDR1_CKE[0]	AN56	DDR_B_CKE0	DDR_B_CKE0	20,21
DDR_A_D22	AK67	DDR1_DQ[5]DDR0_DQ[21]	DDR1_CKE[1]	AP55	DDR_B_CKE1	DDR_B_CKE1	20,21
DDR_A_D23	AK66	DDR1_DQ[6]DDR0_DQ[22]	DDR1_CKE[1]	AN55	DDR_B_CKE2	DDR_B_CKE2	20,21
DDR_A_D24	AF70	DDR1_DQ[7]DDR0_DQ[23]	DDR1_CKE[2]	AP53	DDR_B_CKE3	DDR_B_CKE3	20,21
DDR_A_D25	AF68	DDR1_DQ[8]DDR0_DQ[24]	DDR1_CKE[3]				
DDR_A_D26	AH71	DDR1_DQ[9]DDR0_DQ[25]		BB42	DDR_B_CS#0	DDR_B_CS#0	20,21
DDR_A_D27	AH68	DDR1_DQ[10]DDR0_DQ[26]	DDR1_CS[0]	AY42	DDR_B_CS#1	DDR_B_CS#1	20,21
DDR_A_D28	AF71	DDR1_DQ[11]DDR0_DQ[27]	DDR1_CS[1]	BA42	DDR_B_ODT0	DDR_B_ODT0	20,21
DDR_A_D29	AF69	DDR1_DQ[12]DDR0_DQ[28]	DDR1_ODT[0]	AW42			
DDR_A_D30	AH70	DDR1_DQ[13]DDR0_DQ[29]	DDR1_ODT[1]				
DDR_A_D31	AH69	DDR1_DQ[14]DDR0_DQ[30]		AY48			
DDR_A_D32	AT66	DDR1_DQ[15]DDR0_DQ[31]	DDR1_MA[5]DDR1_CAA[0]DDR1_MA[5]	AP50	DDR_B_CA1_0	DDR_B_CA1_0	20,21
DDR_A_D33	AU66	DDR1_DQ[16]DDR0_DQ[32]	DDR1_MA[6]DDR1_CAA[1]DDR1_MA[6]	BA48	DDR_B_CA1_1	DDR_B_CA1_1	20,21
DDR_A_D34	AP65	DDR1_DQ[17]DDR0_DQ[33]	DDR1_MA[7]DDR1_CAA[2]DDR1_MA[7]	BB48	DDR_B_CA1_2	DDR_B_CA1_2	20,21
DDR_A_D35	AN65	DDR1_DQ[18]DDR0_DQ[34]	DDR1_MA[8]DDR1_CAA[3]DDR1_MA[8]	AP48	DDR_B_CA1_3	DDR_B_CA1_3	20,21
DDR_A_D36	AN66	DDR1_DQ[19]DDR0_DQ[35]	DDR1_MA[9]DDR1_CAA[4]DDR1_MA[9]	BB48	DDR_B_CA1_4	DDR_B_CA1_4	20,21
DDR_A_D37	AP66	DDR1_DQ[20]DDR0_DQ[36]	DDR1_MA[10]DDR1_CAA[5]DDR1_MA[10]	AN50	DDR_B_CA1_5	DDR_B_CA1_5	20,21
DDR_A_D38	AT65	DDR1_DQ[21]DDR0_DQ[37]	DDR1_MA[11]DDR1_CAA[6]DDR1_MA[11]	AN48	DDR_B_CA1_6	DDR_B_CA1_6	20,21
DDR_A_D39	AU65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38]	DDR1_MA[12]DDR1_CAA[7]DDR1_MA[12]	AN53	DDR_B_CA1_7	DDR_B_CA1_7	20,21
DDR_A_D39	AT65	DDR1_DQ[22]DDR0_DQ[38					

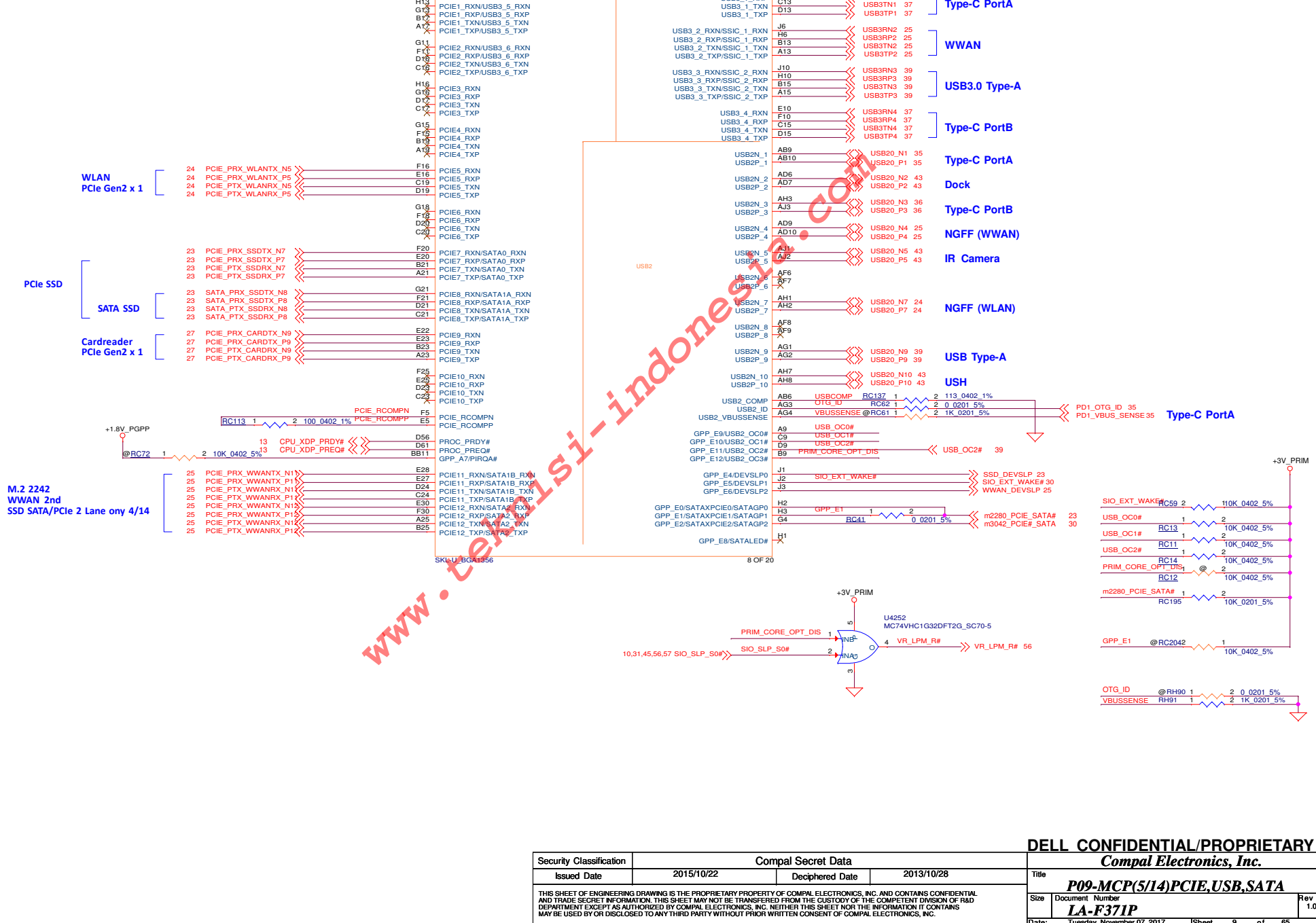


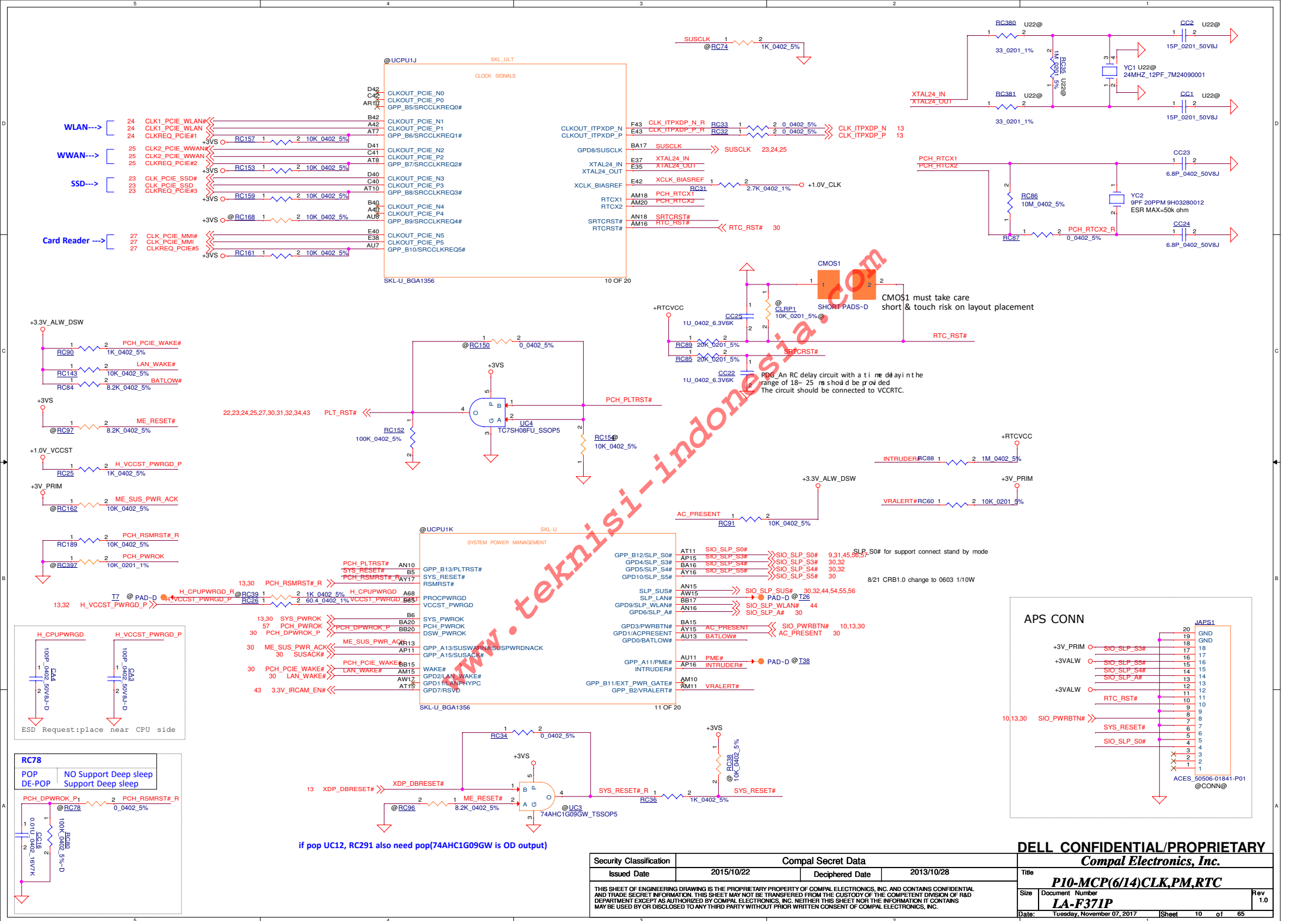
Security Classification	Compal Secret Data	
Issued Date	2015/10/22	Deciphered Date
		2013/10/28

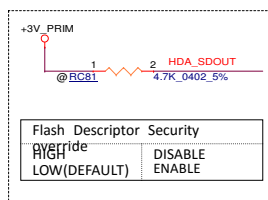
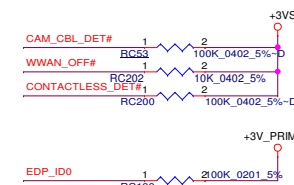
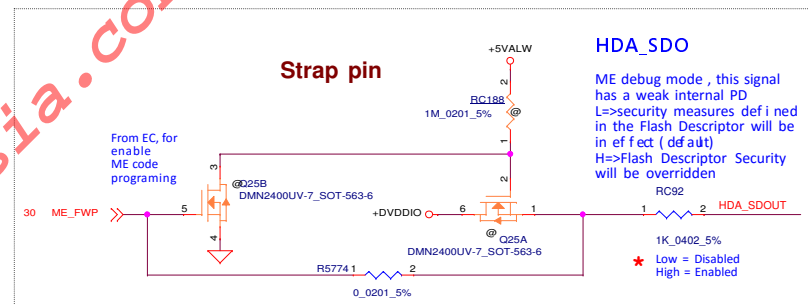
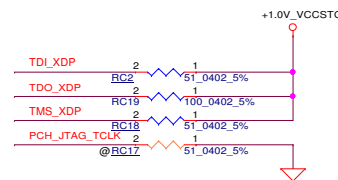
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Size	Document Number	Rev
	LA-F371P	1.0
Date:	Tuesday, November 07, 2017	Sheet 7 of 65





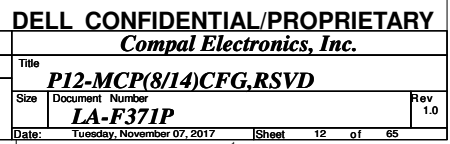


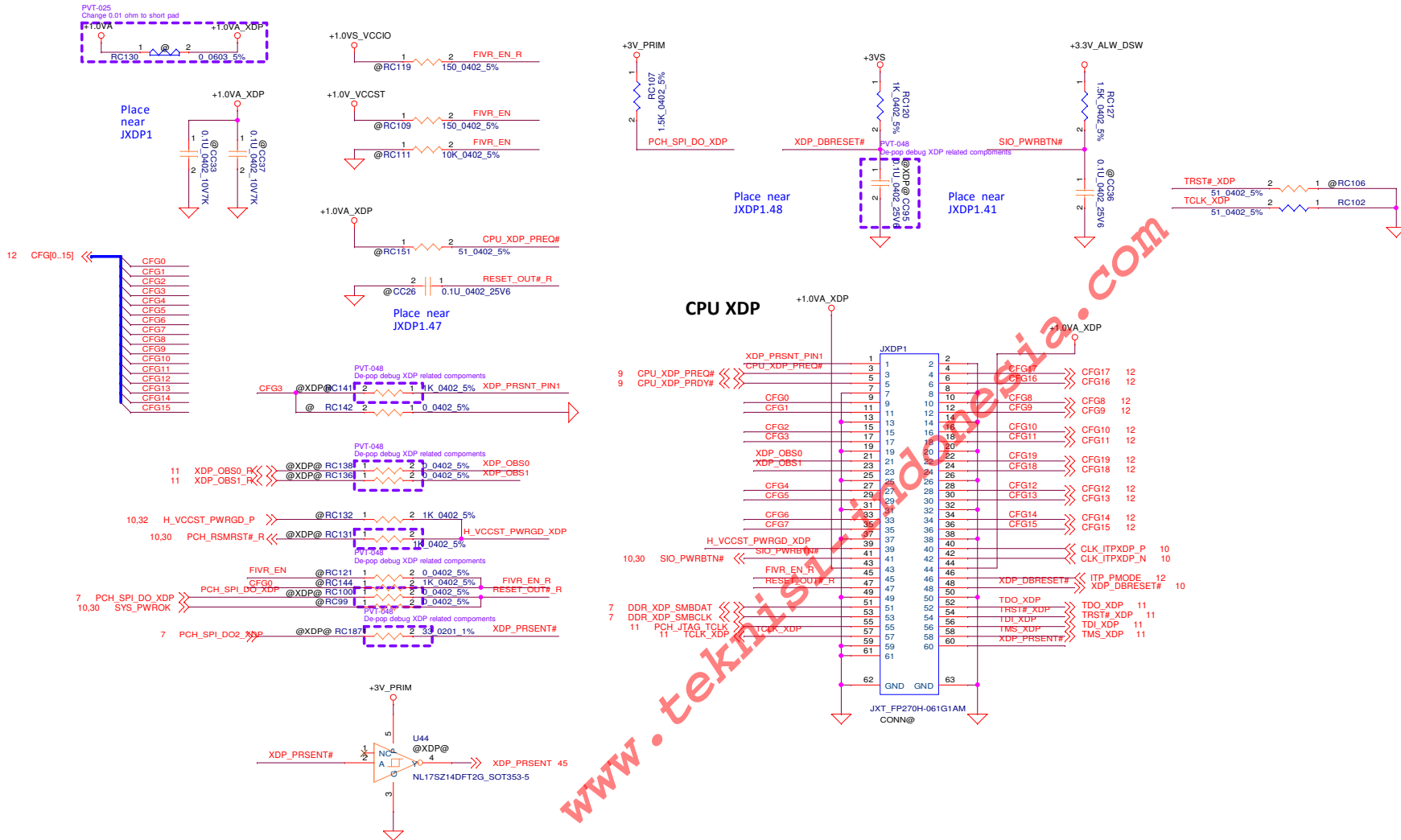


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TPM	1 = W/TPM 0 = W/O TPM

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				Date:	Tuesday, November 07, 2017	Sheet 11 of 65
				LA-F37IP		



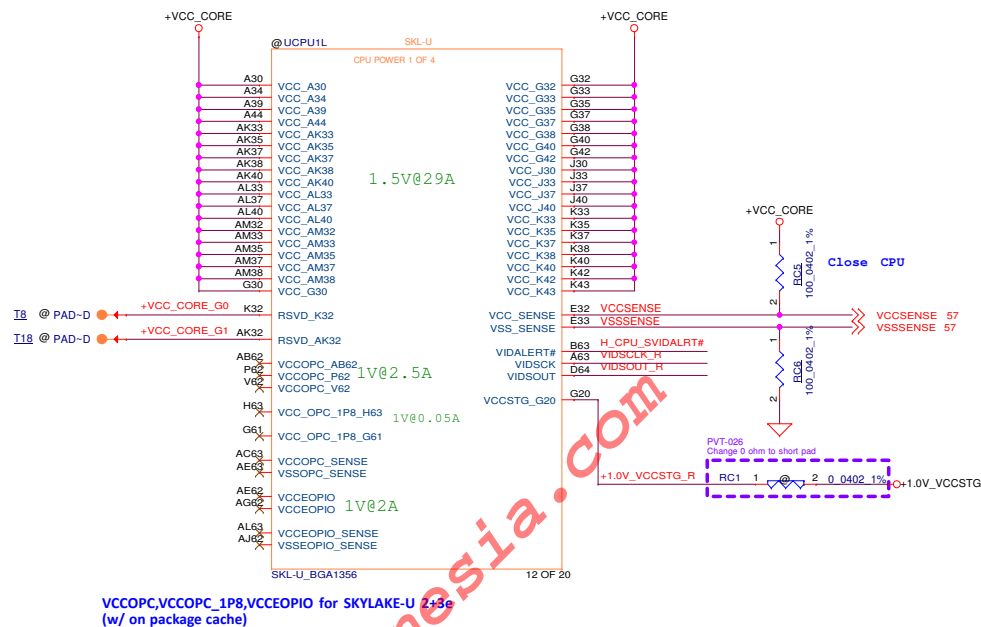


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				Date:	Tuesday, November 07, 2017
				Sheet	13 of 65
				Rev	1.0

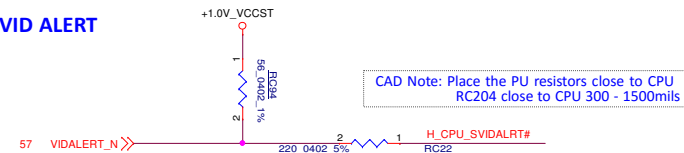
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

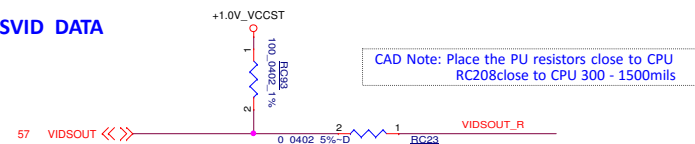
+VCC_CORE: 0.55~1.5V, 29A
+VCC_EDRAM: 1V, 2.5A
+V1.8S_EDRAM: 1.8V, 50mA
+VCC_EOPIO: 0.8~1V, 2A



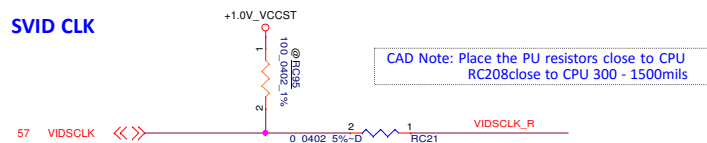
SVID ALERT



SVID DATA



SVID CLK



CDI#61280

10.2.7 SVID Topology

Table 10-9. SVID Bus Routing Guidelines

need double pull high

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					LA-F371P	1.0
				Date:	Tuesday, November 07, 2017	Sheet 14 of 65

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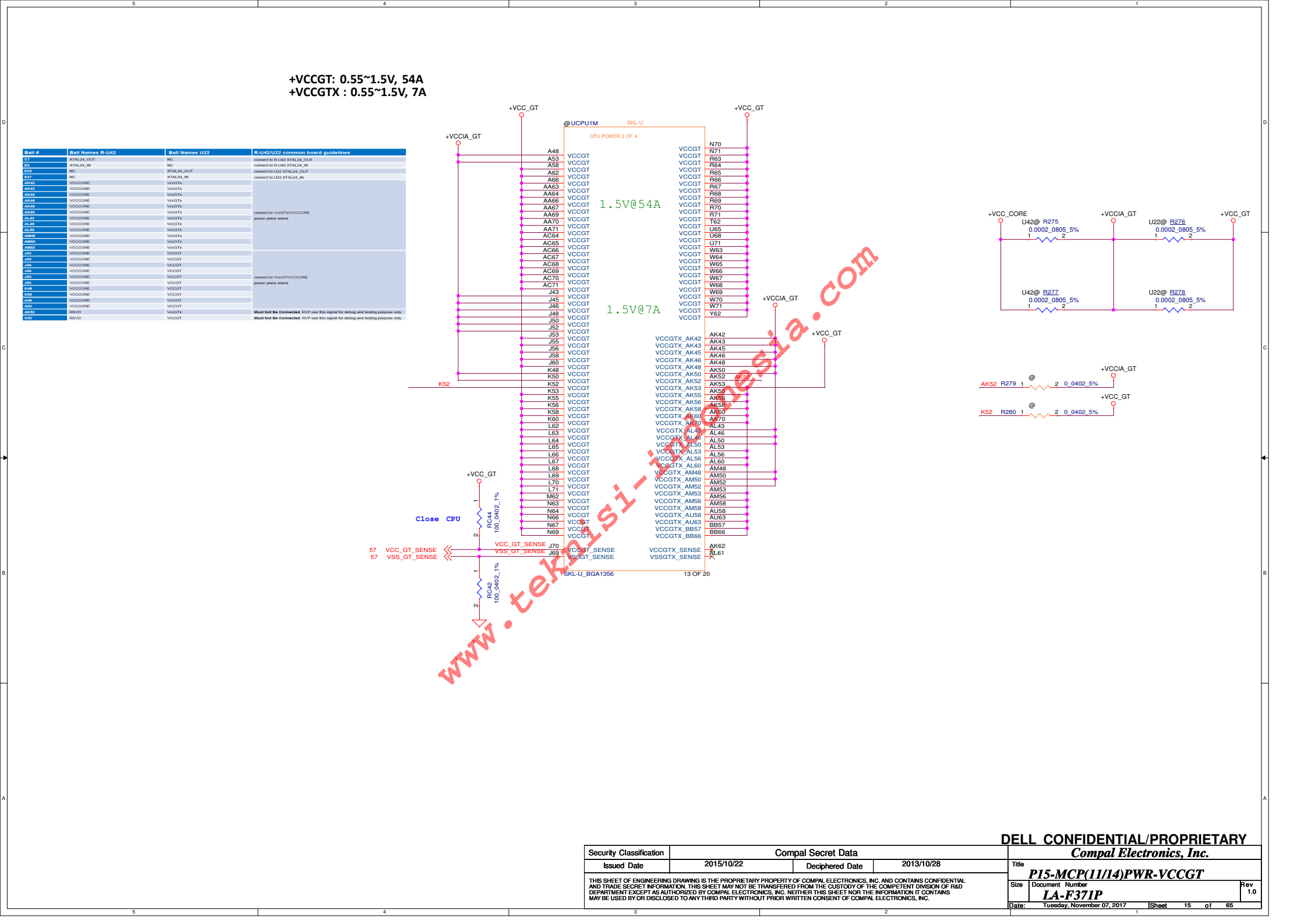
517

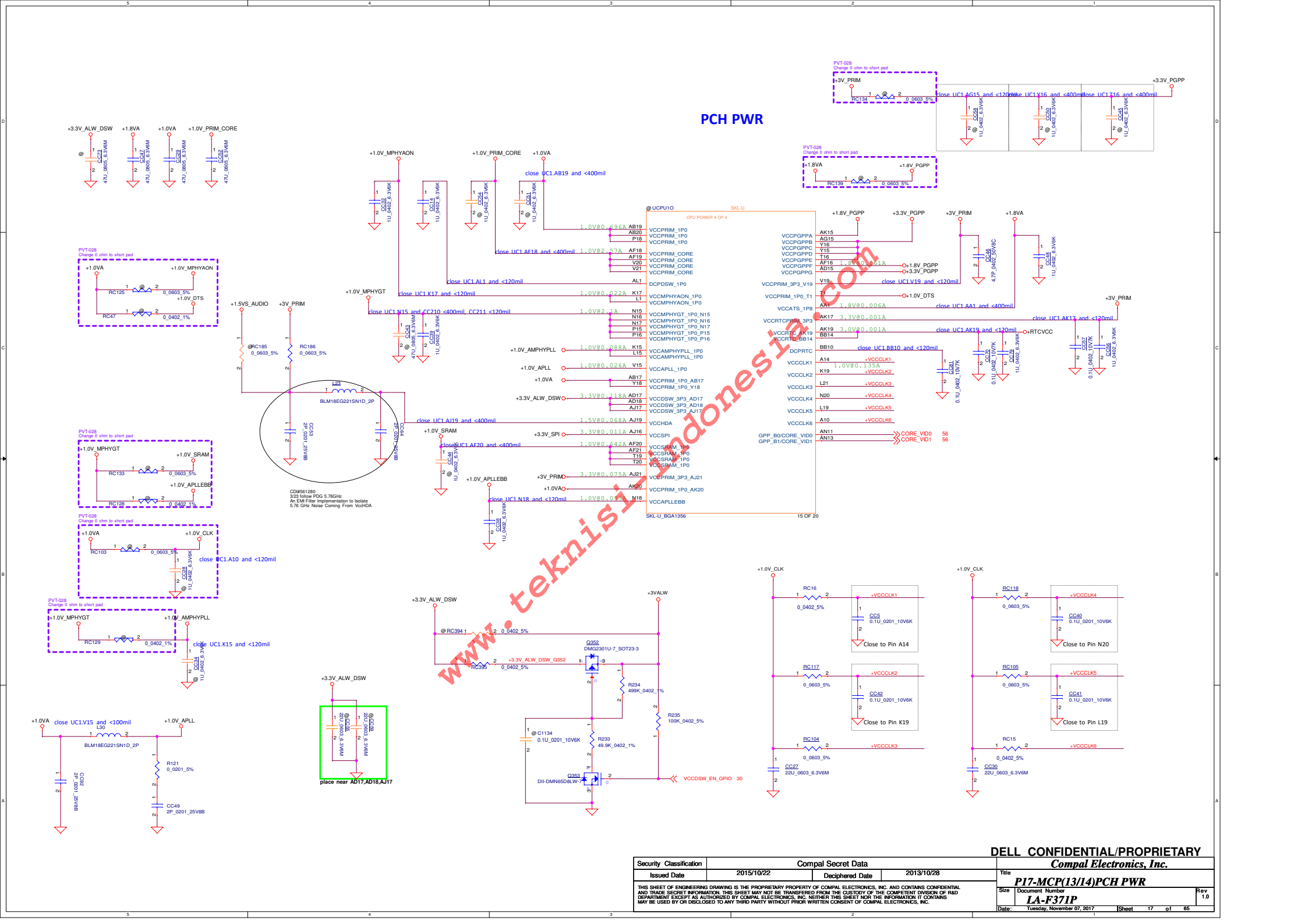
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<

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PCH PWR

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				Date: Tuesday, November 07, 2017 Sheet 17 of 65

Note1: VCCPRIM_CORE Implementat i on wá h PCH CORE_V D Reco mnendat i on

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424

@UCPU1P SKL-U

GND 1 OF 3

@UCPU1Q SKL-U

GND 2 OF 3

@UCPU1R SKL-U

GND 3 OF 3

A5 VSS
A67 VSS
A70 VSS
AA2 VSS
AA4 VSS
AA65 VSS
AB68 VSS
AB15 VSS
AB16 VSS
AB18 VSS
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AD13 VSS
AD16 VSS
AD19 VSS
AD20 VSS
AD21 VSS
AD62 VSS
AD8 VSS
AE64 VSS
AE65 VSS
AE66 VSS
AE67 VSS
AE68 VSS
AE69 VSS
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BB64 VSS
BB67 VSS
BB70 VSS
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D10 VSS
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SKL-U_BGA1356 18 OF 20

SKL-U_BGA1356 16 OF 20

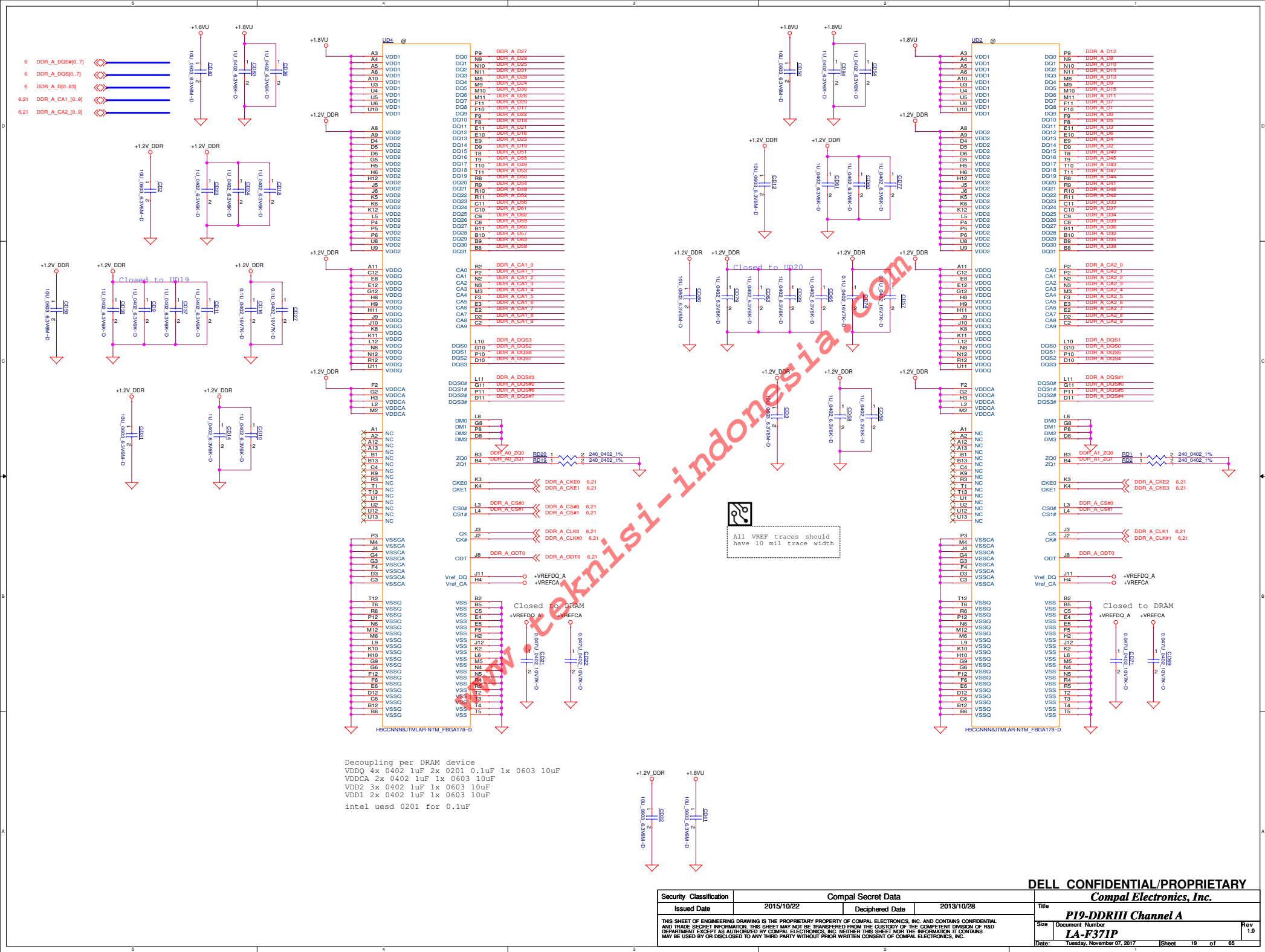
SKL-U_BGA1356 17 OF 20

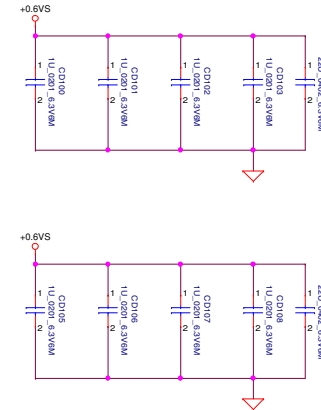
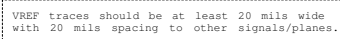
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				Date:	Rev
				Tuesday, November 07, 2017	1.0
				Sheet	18 of 65



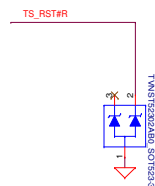


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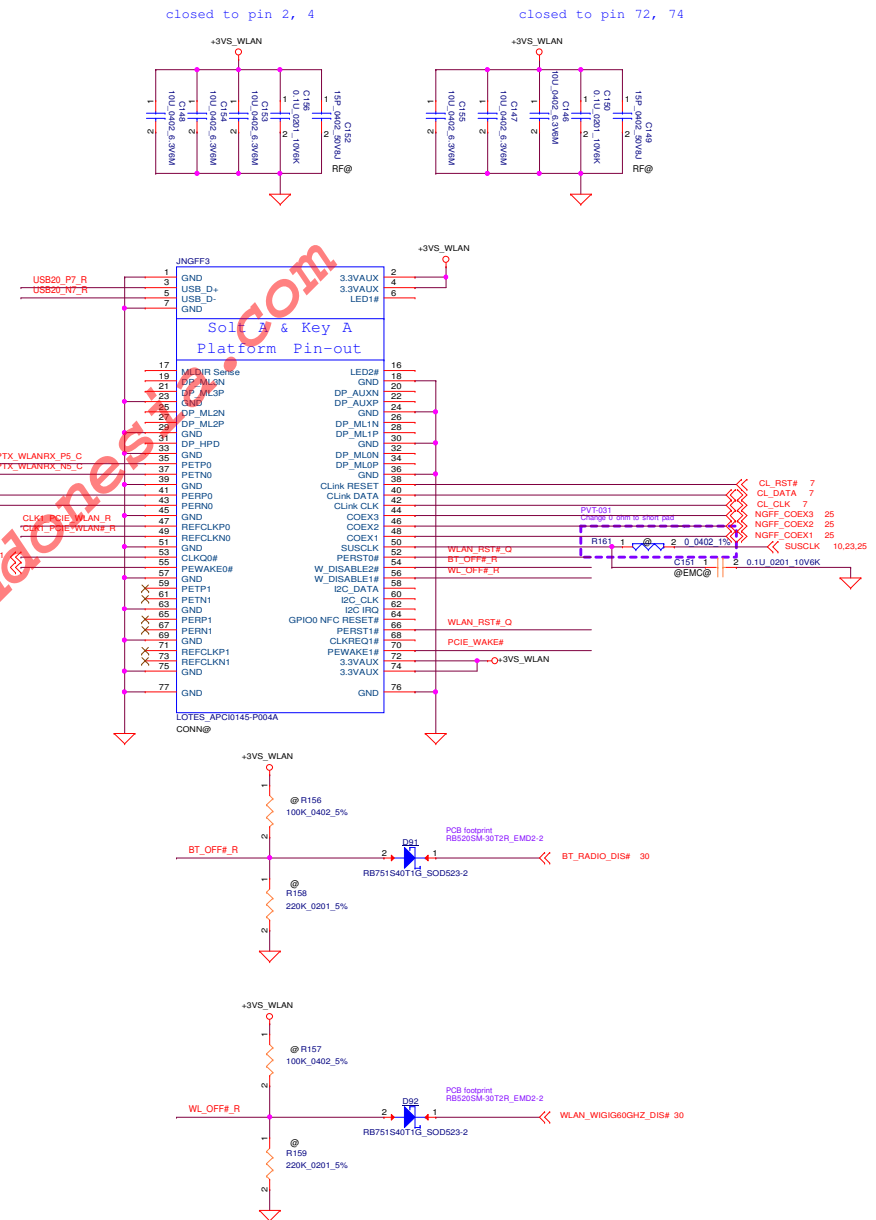
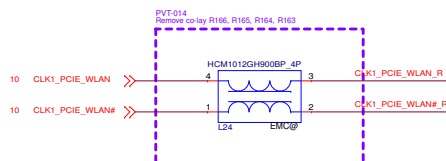
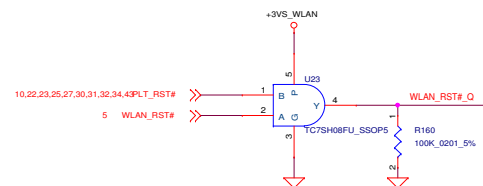
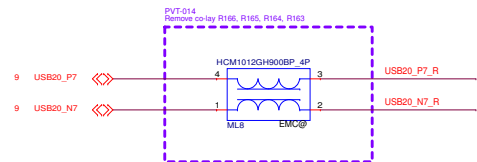
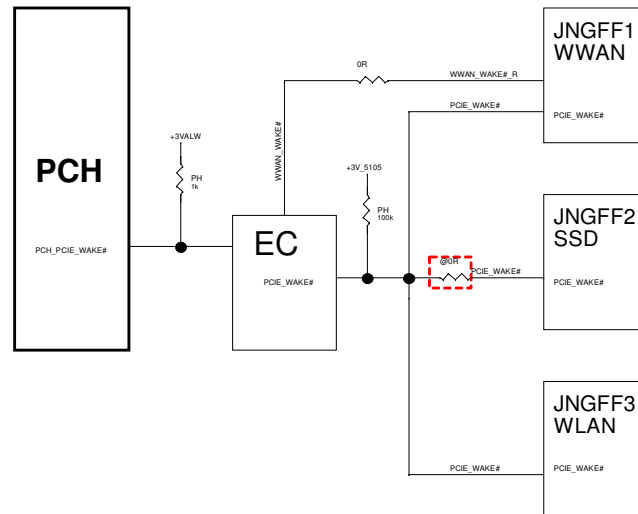


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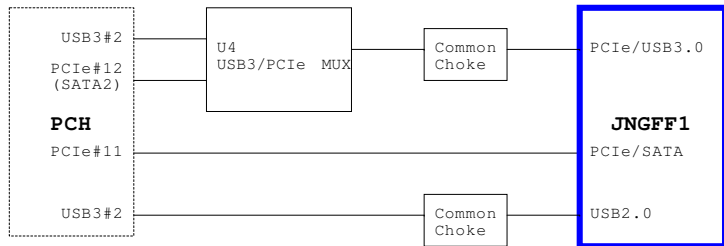


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				LA-F371P		
				Date:	Tuesday, November 07, 2017	Sheet 22 of 65

Wireless LAN



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Date:		Tuesday, November 07, 2017		Sheet		24 of 65				



PCIe/USB 3.0 Mux

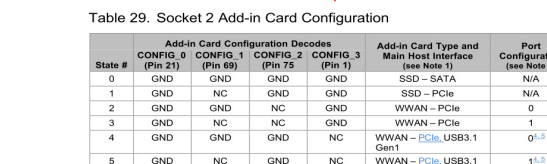
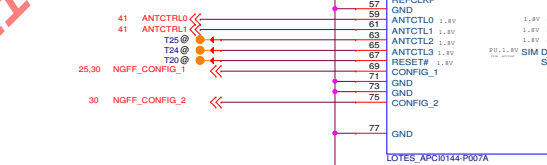
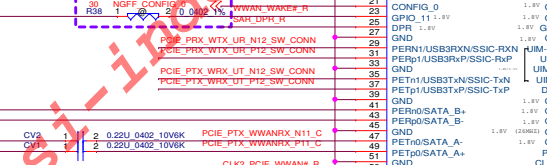
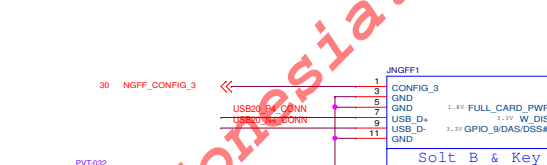
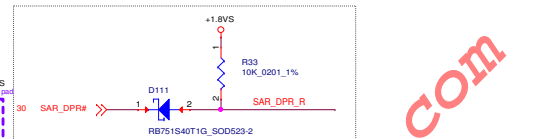
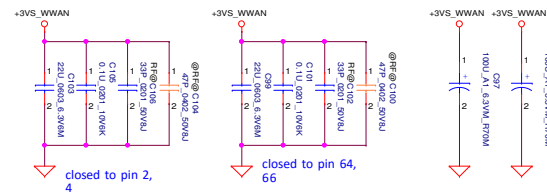
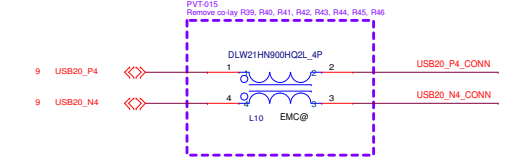
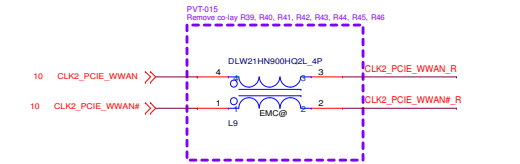
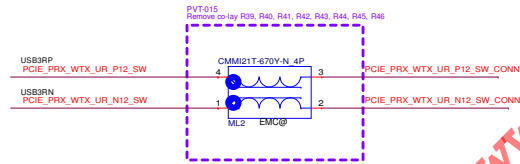
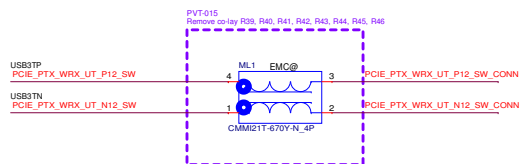
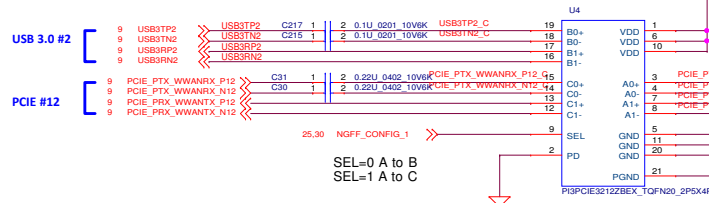
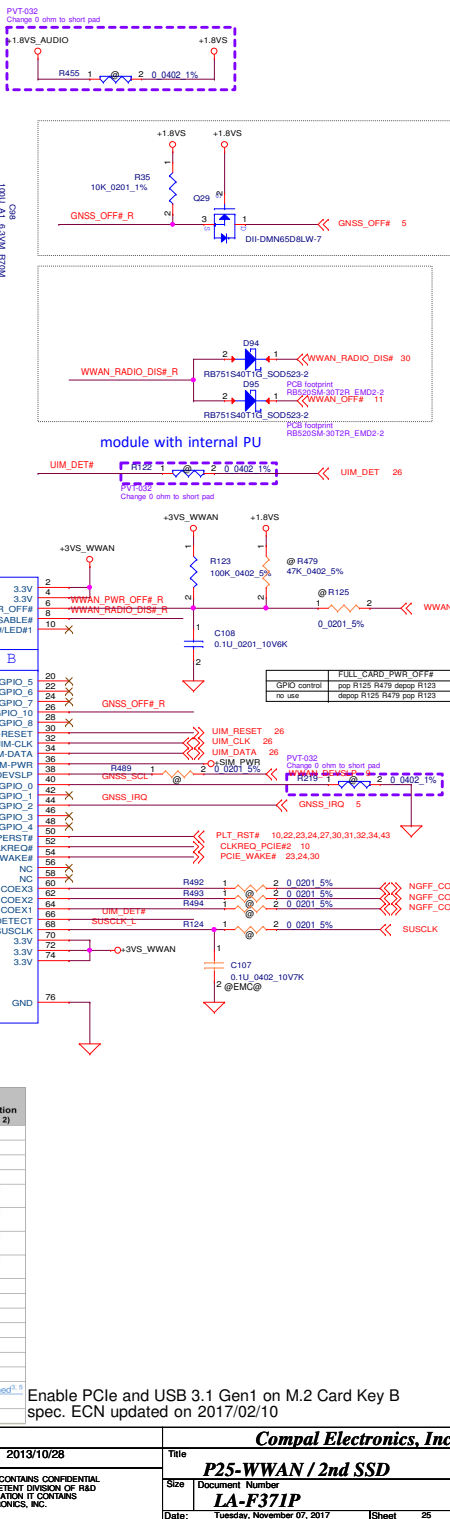


Table 29. Socket 2 Add-in Card Configuration

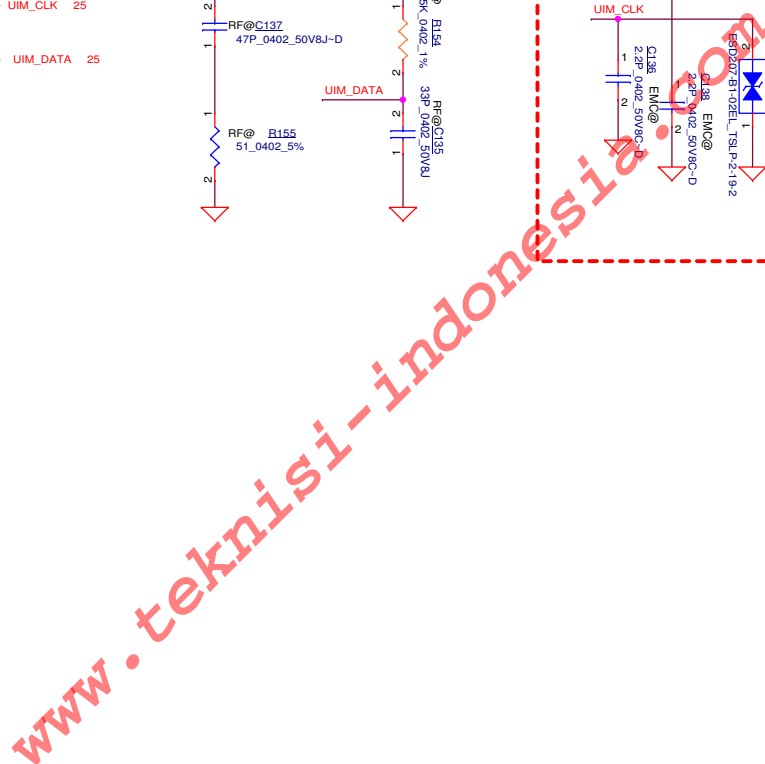
State #	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Add-in Card Type and Main Host Interface (see Note 1)	Port Configuration (see Note 2)
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	NC	GND	GND	SSD - PCIe	N/A
2	GND	NC	NC	GND	WWAN - PCIe	0
3	GND	NC	NC	GND	WWAN - PCIe	1
4	GND	NC	GND	NC	WWAN - PCIe, USB3.1 Gen1	0 ^{1,5}
5	GND	NC	GND	NC	WWAN - PCIe, USB3.1 Gen1	1 ^{1,5}
6	GND	GND	NC	NC	WWAN - PCIe, USB3.1 Gen1	2 ^{1,5}
7	GND	NC	NC	NC	WWAN - PCIe, USB3.1 Gen1	3 ^{1,5}
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	NC	GND	GND	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	NC	NC	GND	WWAN - SSIC	3
12	NC	GND	GND	NC	WWAN - PCIe	0
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	GND	NC	NC	WWAN - PCIe, USB3.1 Gen1	N/A
15	NC	NC	NC	NC	No Add-in Card Present	N/A



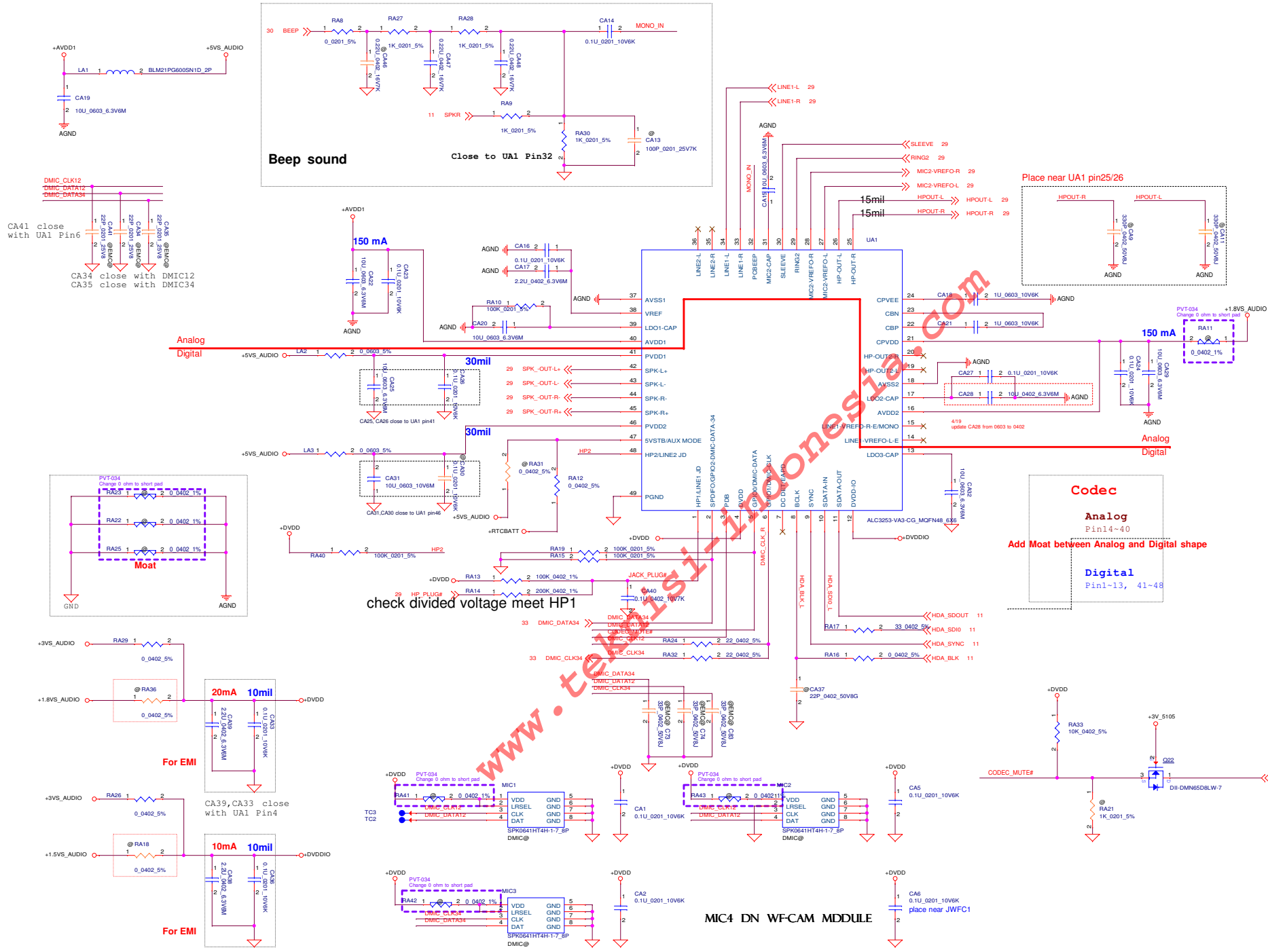
Enable PCIe and USB 3.1 Gen1 on M.2 Card Key B spec. ECN updated on 2017/02/10

The left diagram shows the RF input and output connections. The input is labeled RF@C137, 47P_0402_50V8J-D. The output is labeled RF@C135, 33P_0402_50V8J. The input is connected to a 1% resistor R154. The output is connected to a 5% resistor R155. The input and output are connected to a 50V8J-D device.

The right diagram shows the UIM_CLK and UIM_DATA connections. The UIM_CLK is connected to a 2.2P_0402_50V8C-D device. The UIM_DATA is connected to a 2.2P_0402_50V8C-D device. The UIM_CLK and UIM_DATA are connected to a 50V8J-D device.



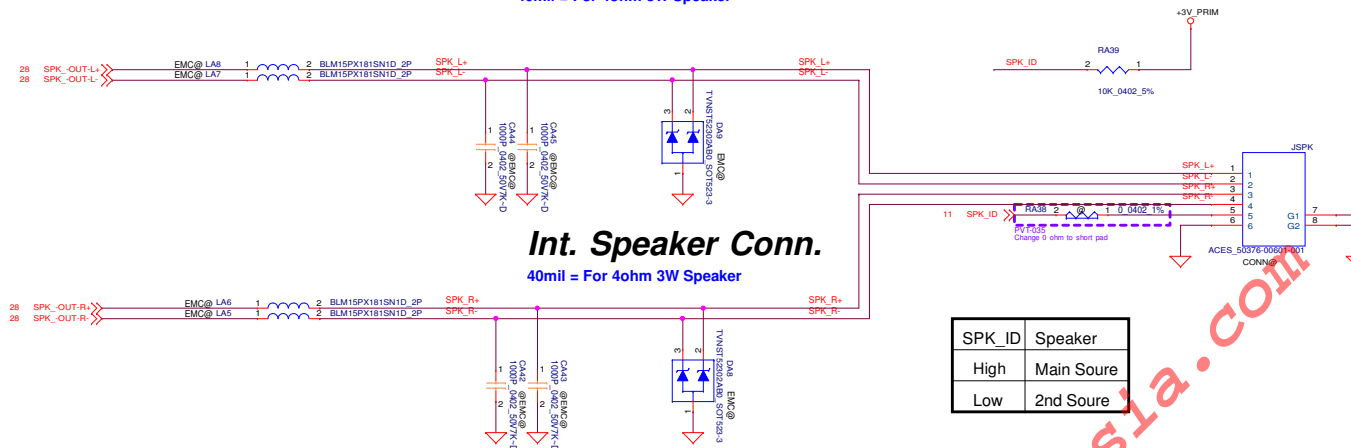
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				Date:	Tuesday, November 07, 2017	Sheet	26 of 65



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Size		Document Number				Rev 1.0
		LA-F371P				
Date:		Tuesday, November 07, 2017			Sheet 28 of 65	

Int. Speaker Conn.

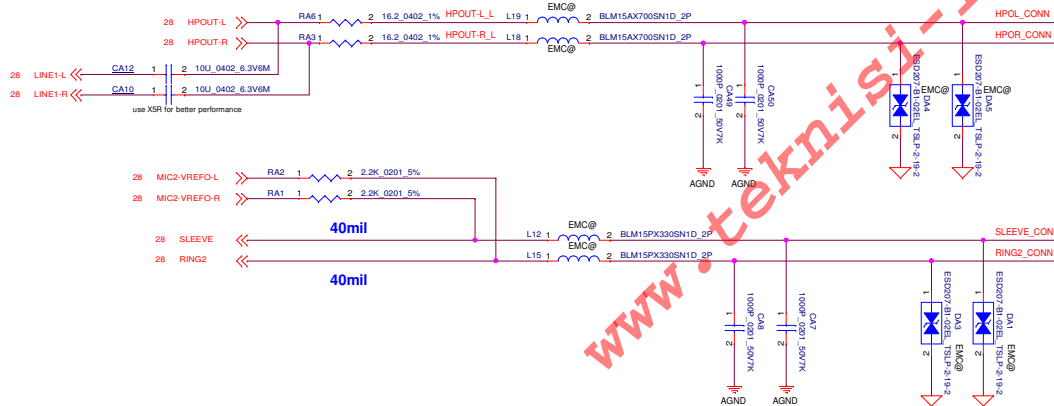
40mil = For 4ohm 3W Speaker



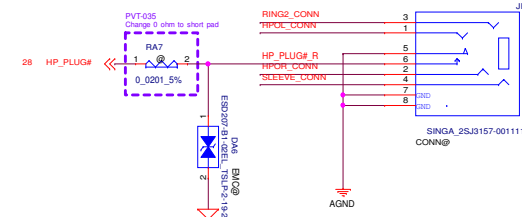
Int. Speaker Conn.

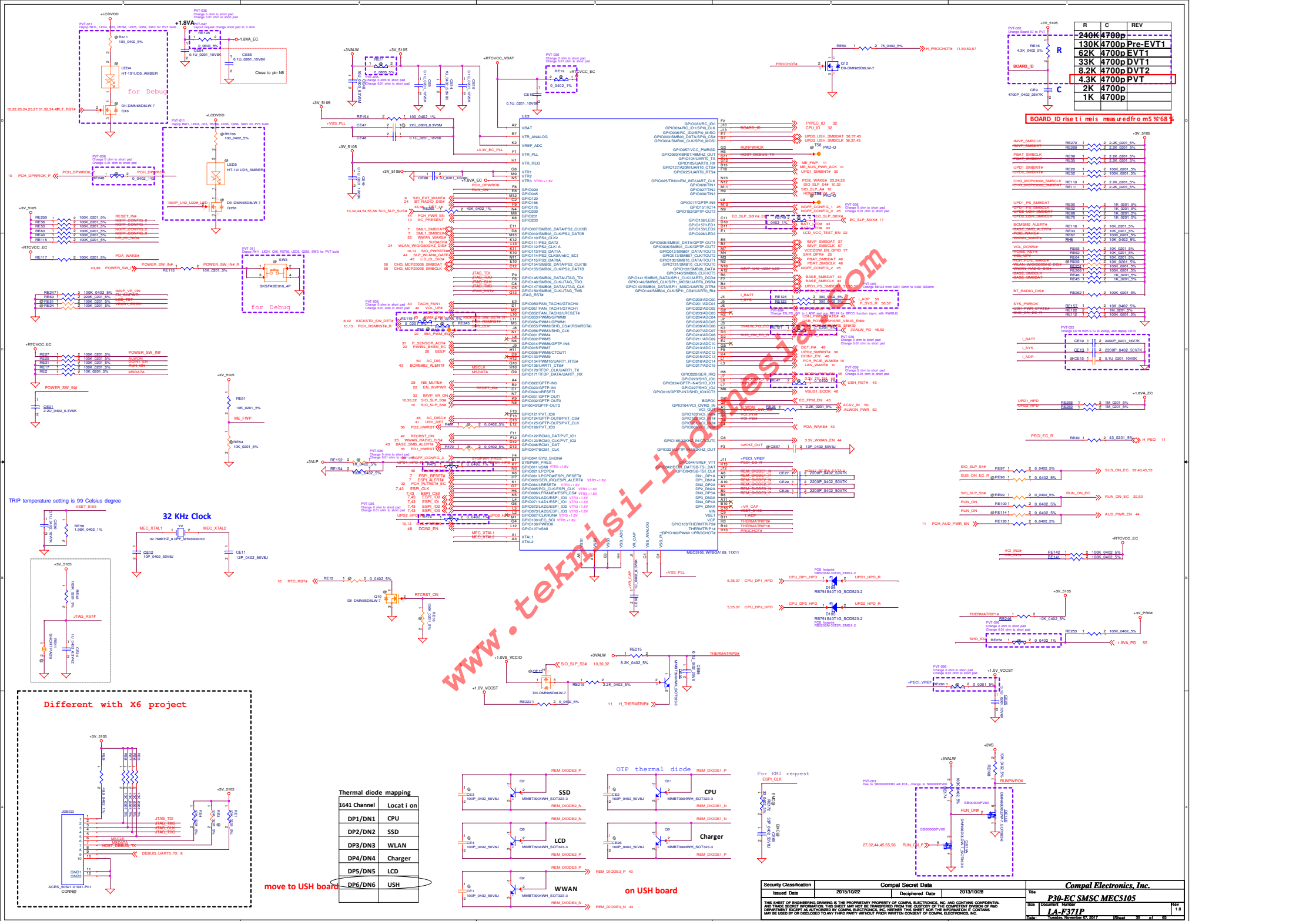
40mil = For 4ohm 3W Speaker

Universal Audio Jack

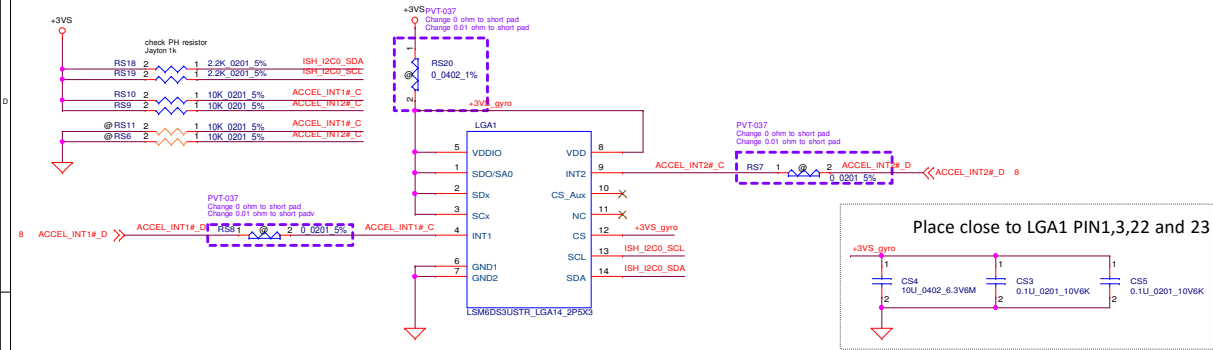


Universal Audio Jack CONN



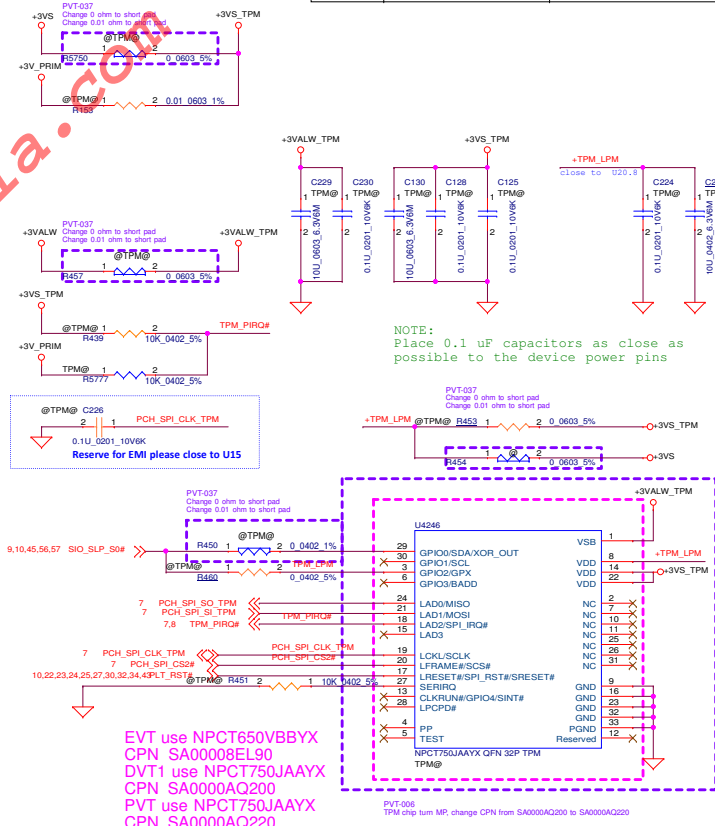


Gyro + Accelerometer

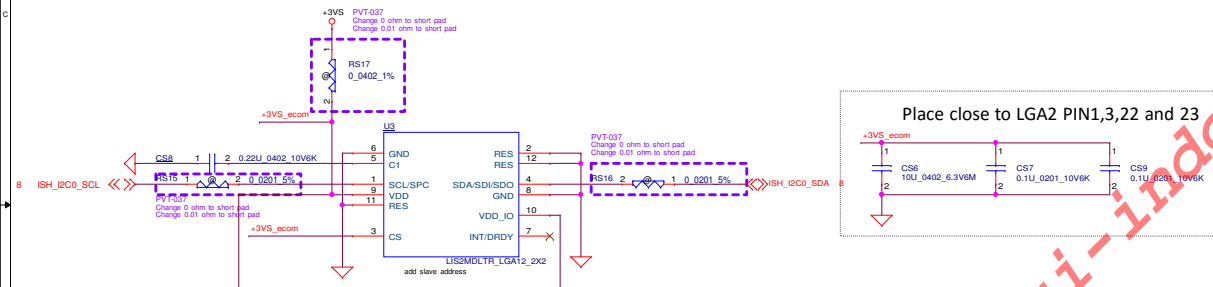


TPM

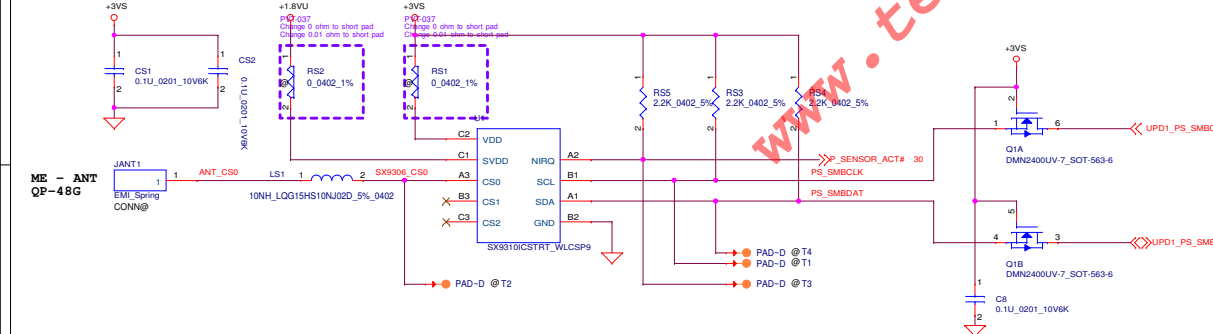
	Pop	De-pop
NPCT65x	R153, R451, R460	R5750, R450
NPCT75x	R5750, R450	R153, R451, R460

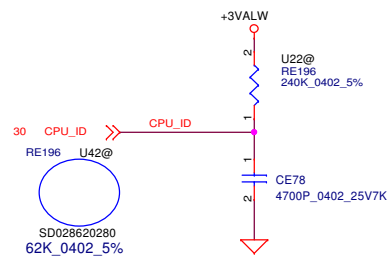
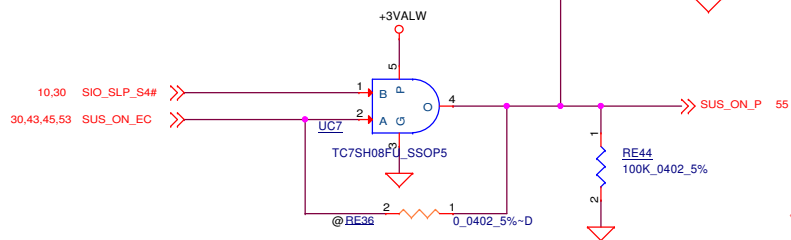
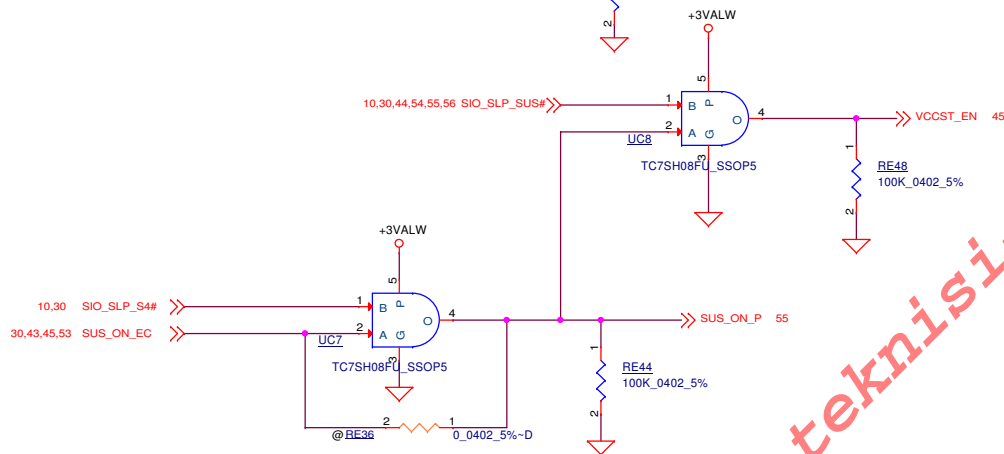
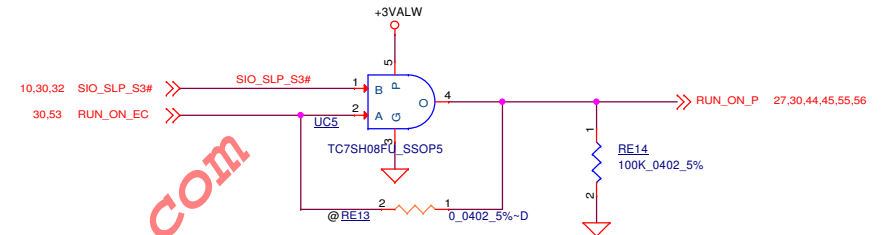
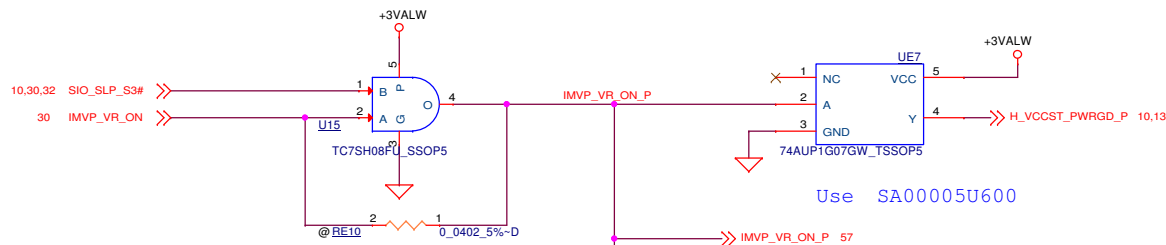
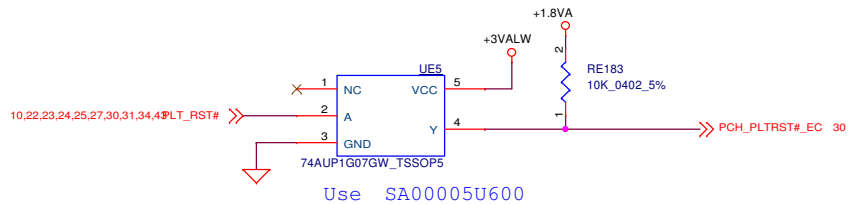


E-Compass

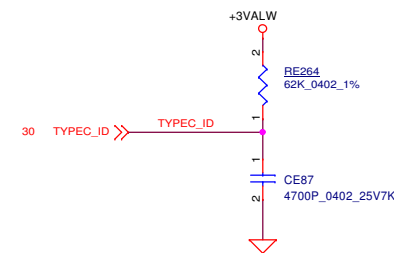


SAR Proximity Sensor



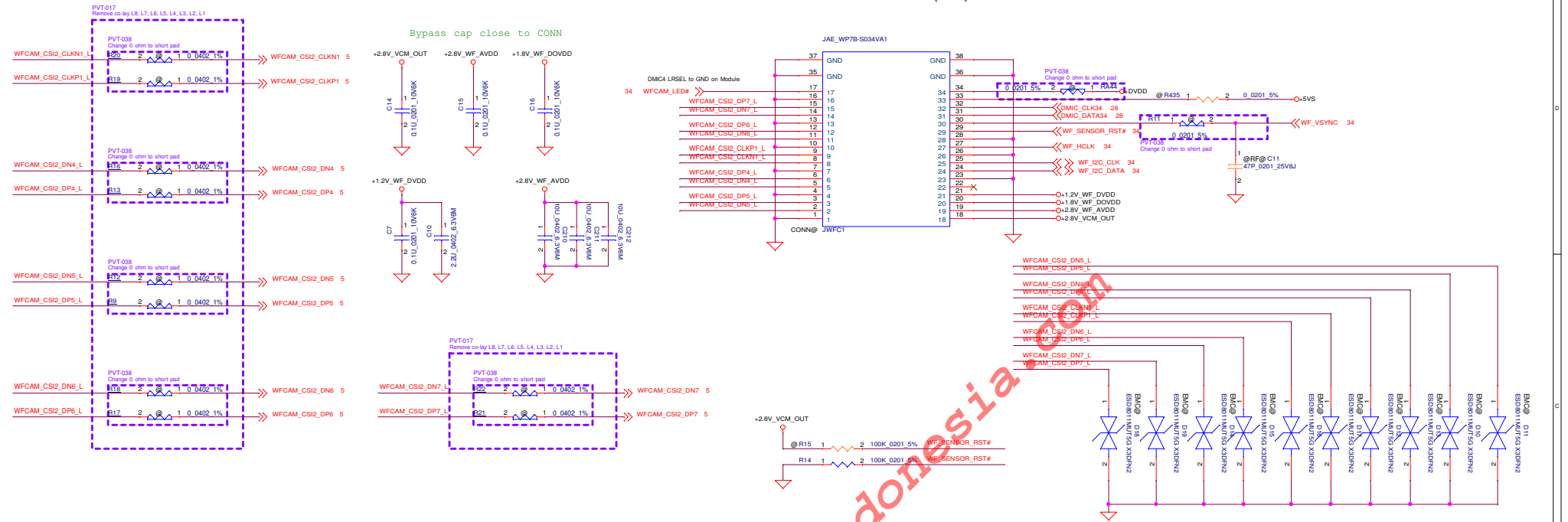


RE196	CE78	REV
240K	4700p	U2+2
130K	4700p	
62K	4700p	U4+2
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

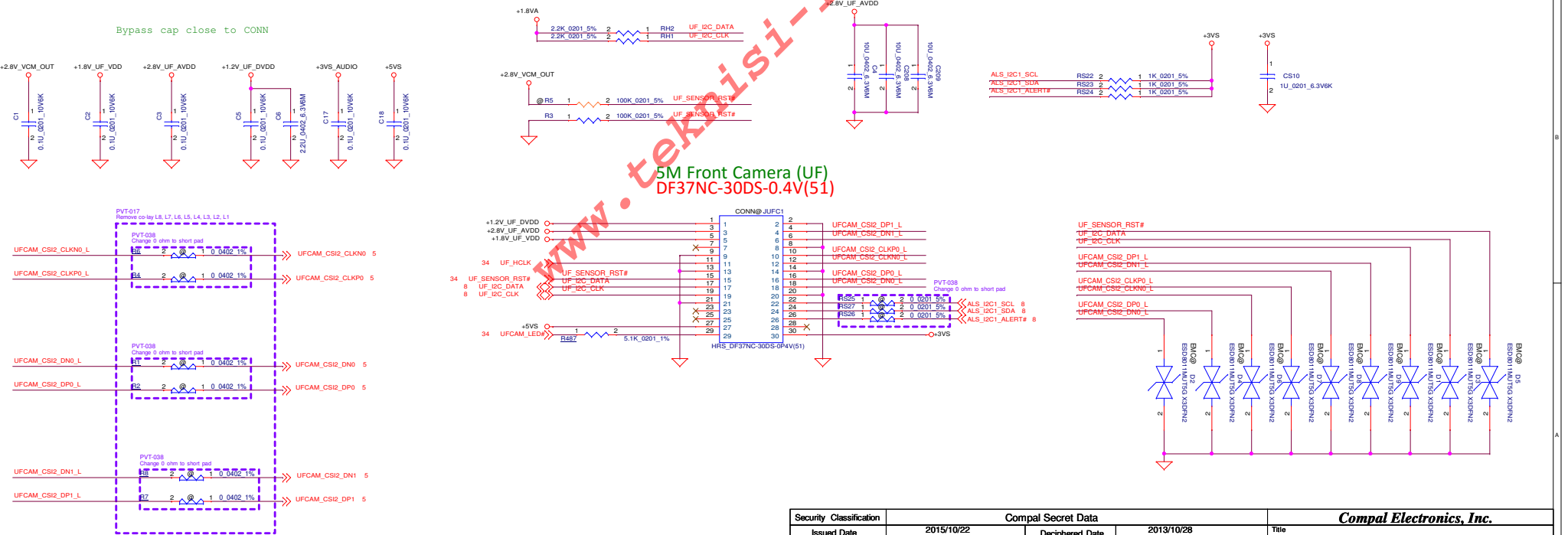


RE264	CE87	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/ AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/ AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	

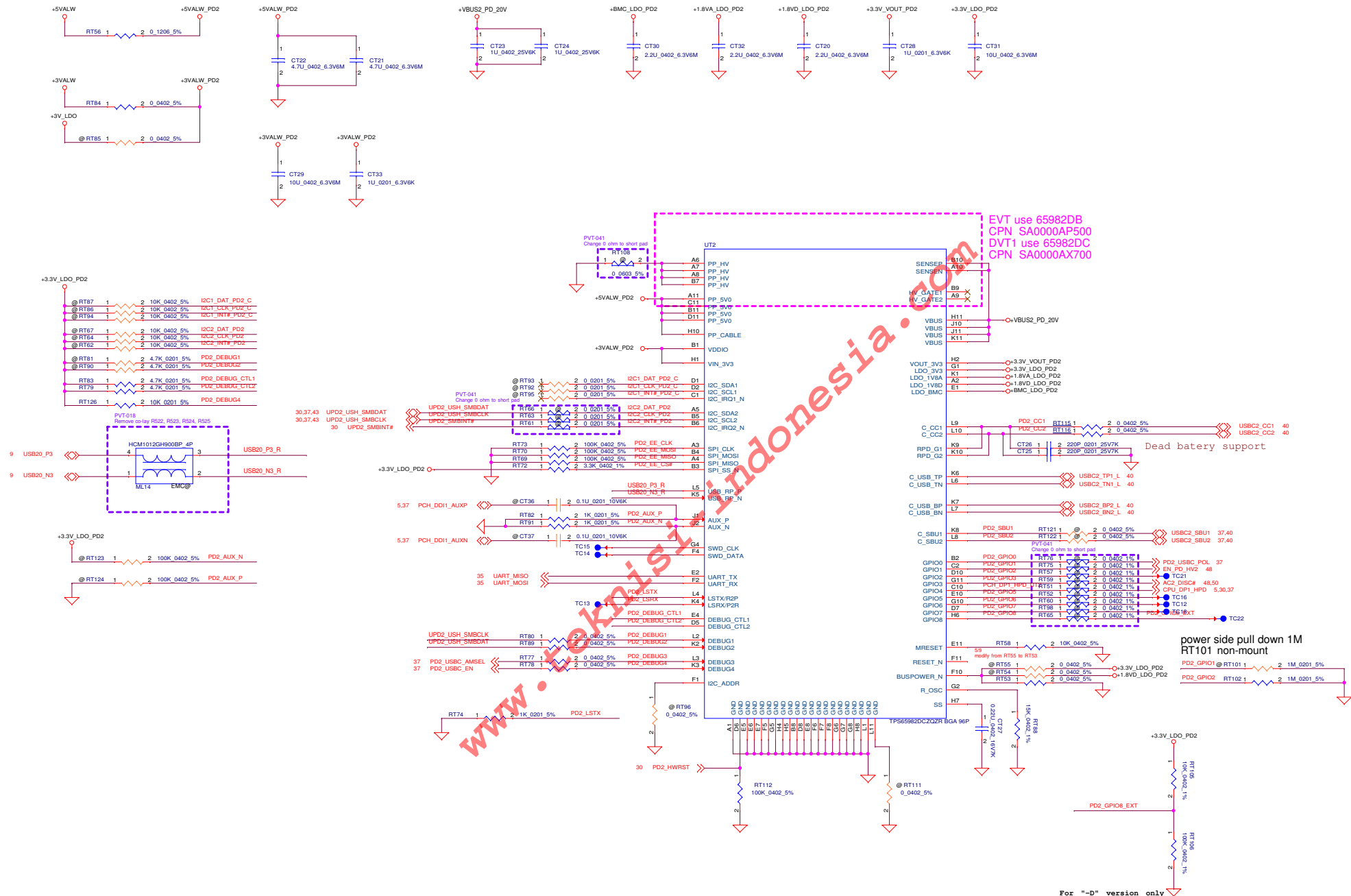
8M Rear Camera (WF)



5M Front Camera (UF)
DF37NC-30DS-0.4V(51

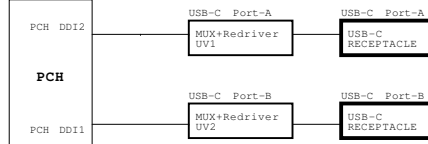


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				Size	Document Number	Rev
				LA-F371P		
Date: Tuesday, November 07, 2017				Sheet	33	of 65



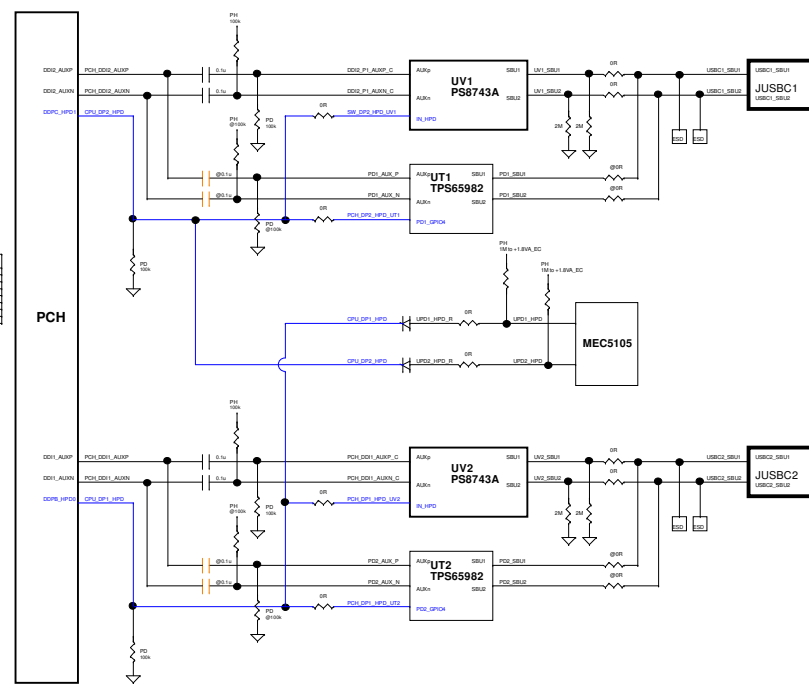
For "-D" version only
 Factory Set Device Configurations 7
 Infinite boot retry from Flash to Host I/F cycles.
 DIV=RT106/(RT105+RT106)
 between 0.7-1.0

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				P36-PD Controller TI	
				Size	Document Number
				C	LA-F371P
				Date:	Tuesday, November 07, 2017
				Sheet	36 of 65

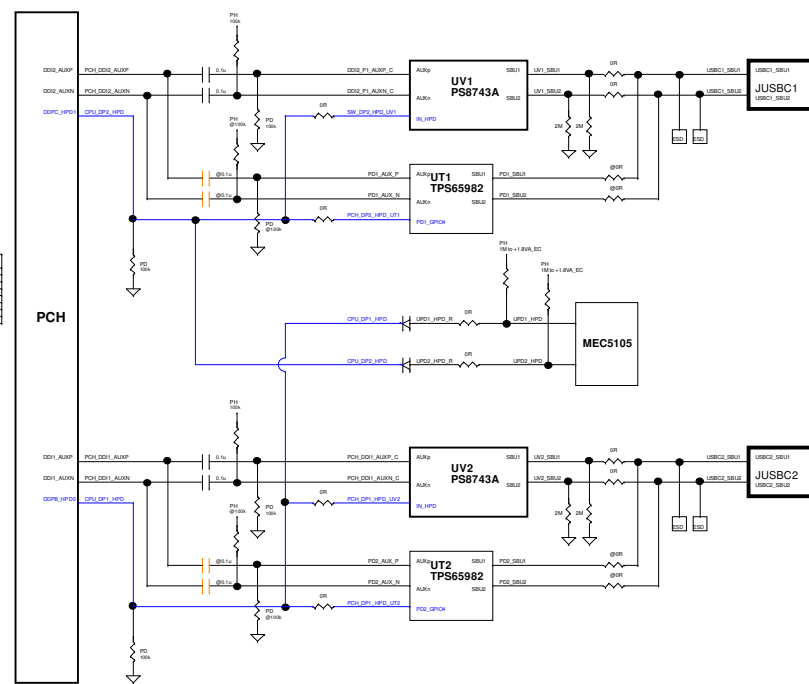


USBC1 MUX default H/W setting

USB 3.0 AC Coupling Capacitor Topolog

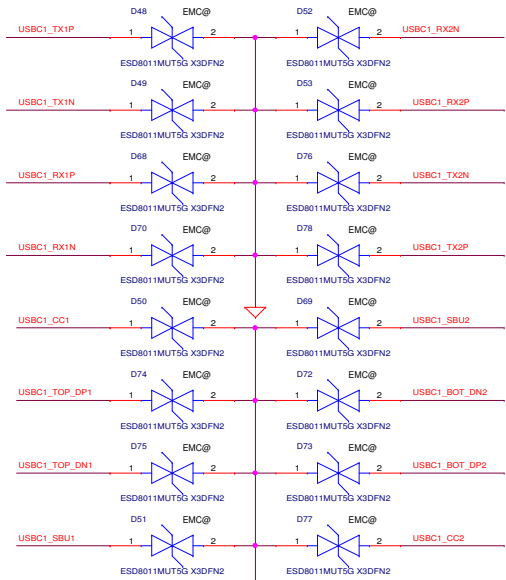
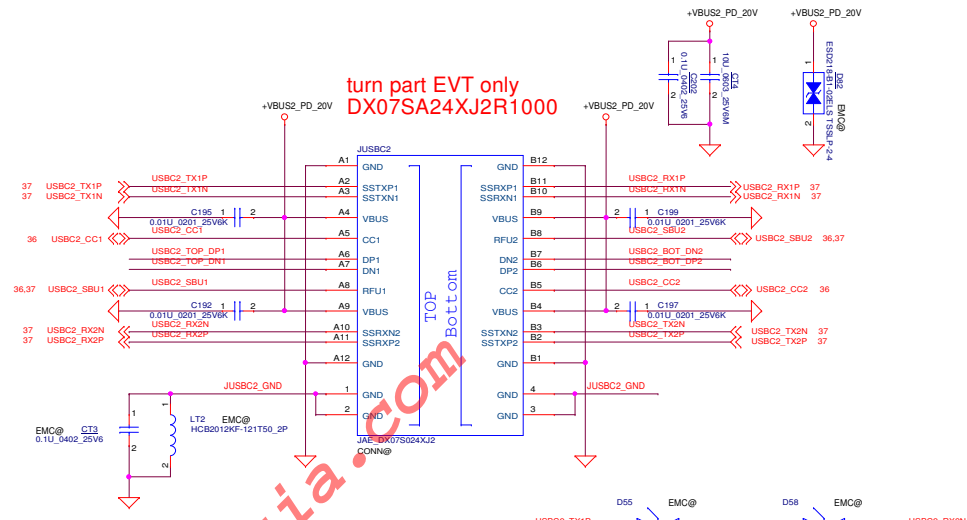
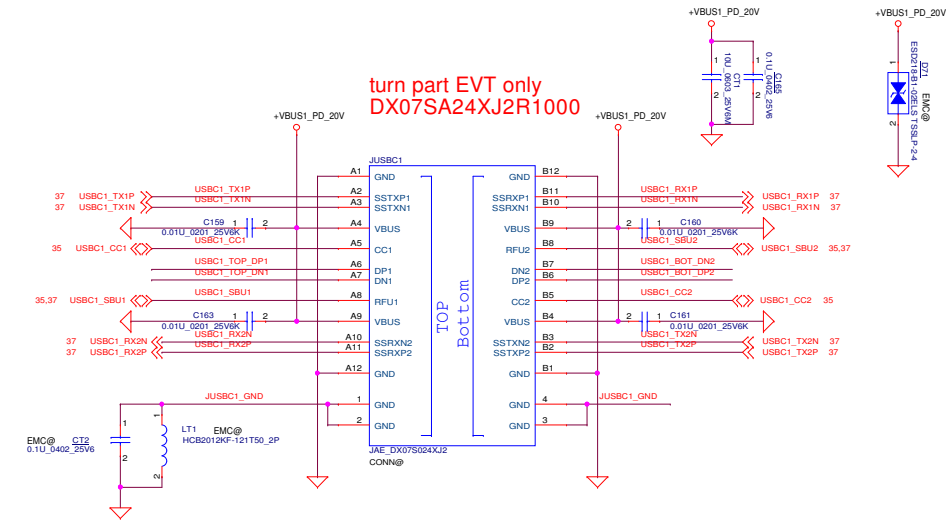


USBC2 MUX default H/W setting



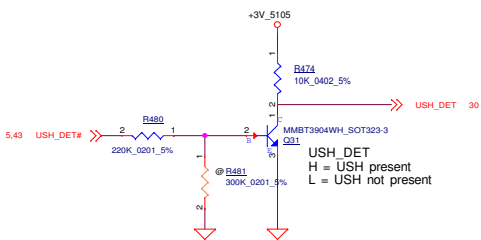
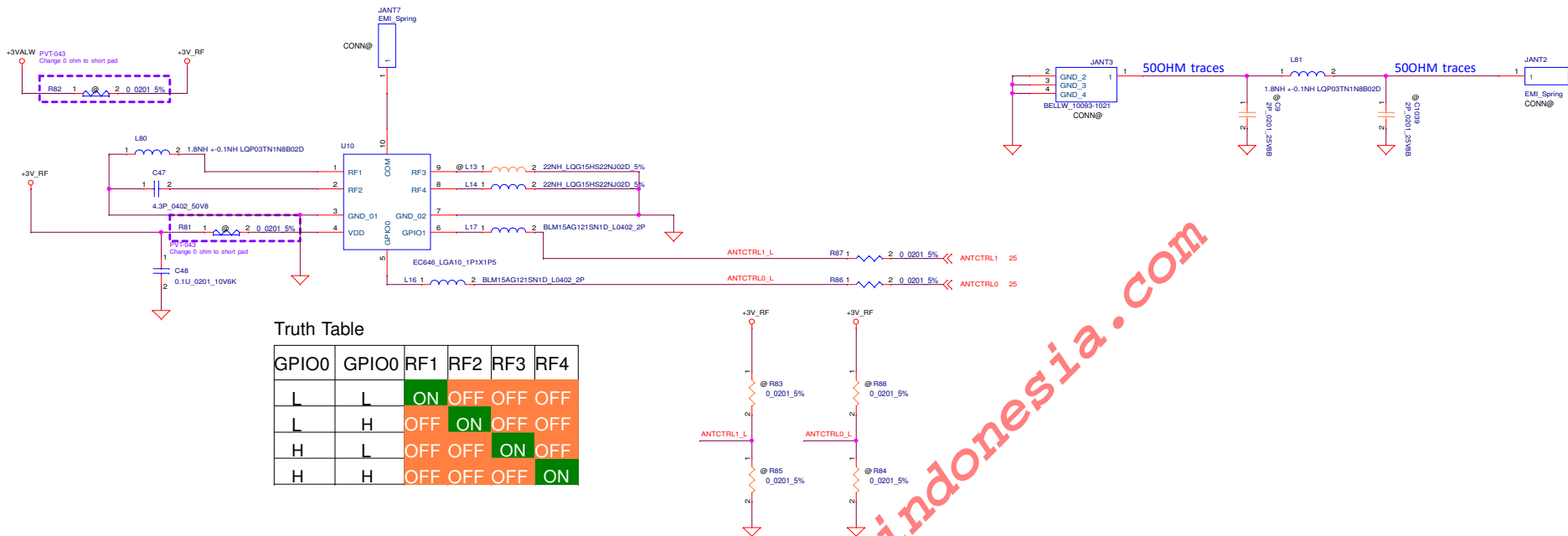
www.teknisi-indonesia.com

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				C	LA-F371P	1.0
				Date:	Tuesday, November 07, 2017	Sheet 38 of 65

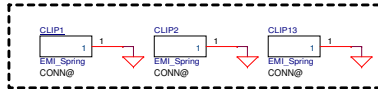
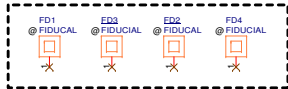


Tunable IC

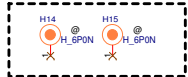
RF conn for WWAN



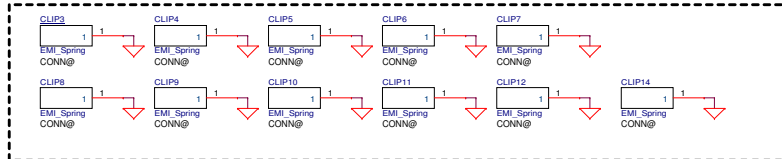
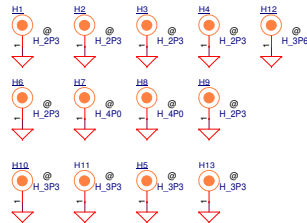
SCREW HOLE



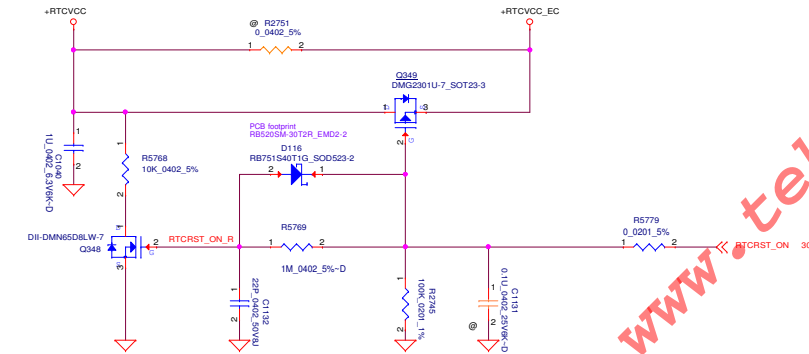
for cable routing



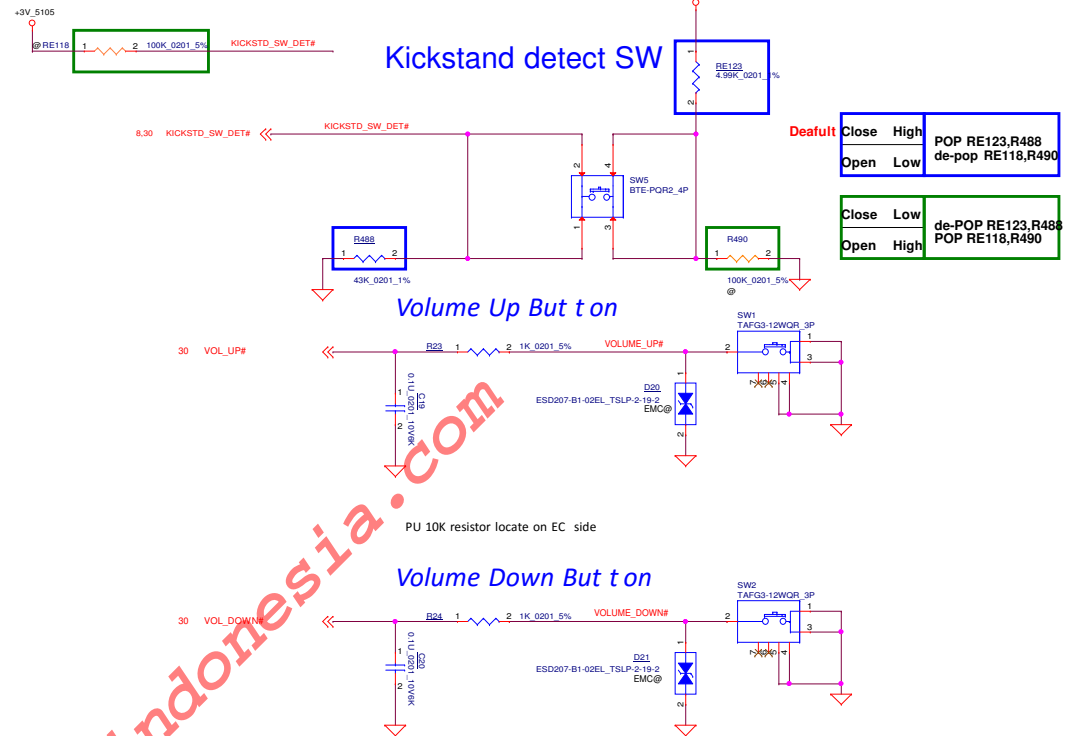
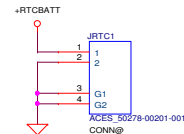
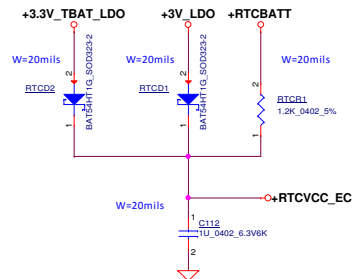
for WLAN/WWAN



for M.2 SSD/WLAN/WWAN shielding clip



RTC



Kickstand detect SW

Close High POP RE123,R488
Open Low de-pop RE118,R490

Close Low de-POP RE123,R488
Open High POP RE118,R490

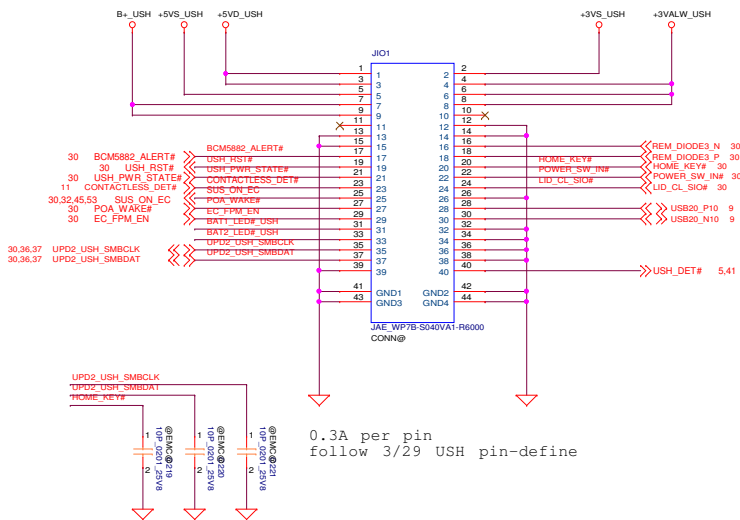
Volume Up But t on

Volume Down But t on

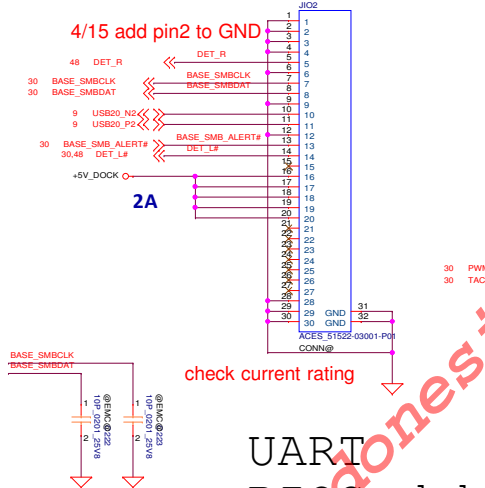
SATA LED

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				LA-F371P	Rev 1.0
				Date:	Tuesday, November 07, 2017
				Sheet	42 of 65

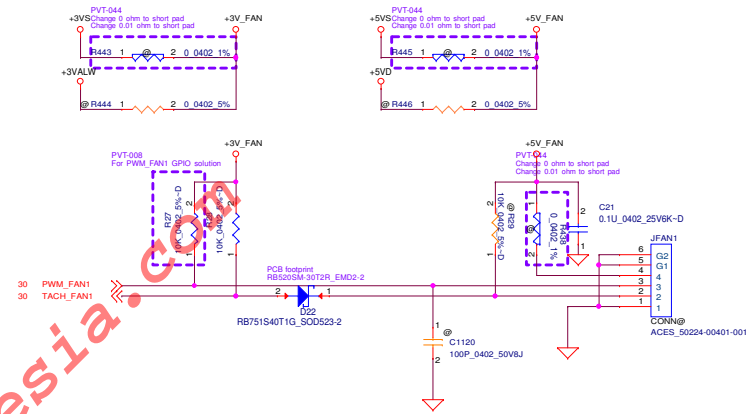
USH CONN



Docking CONN



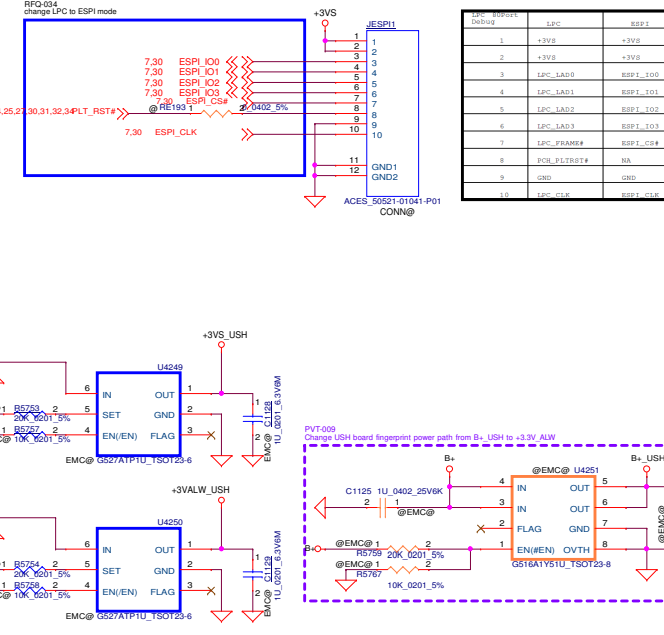
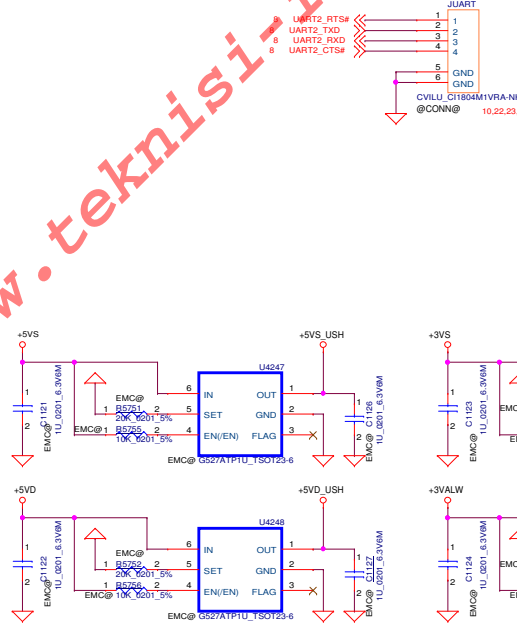
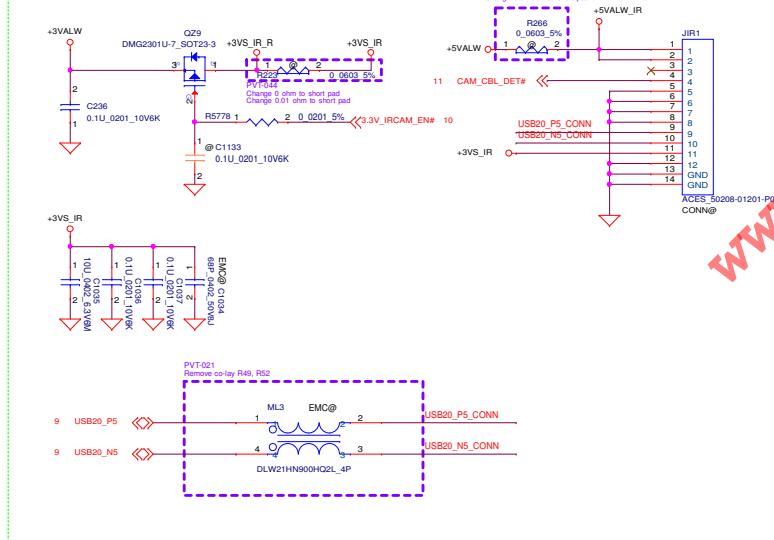
FAN CONN



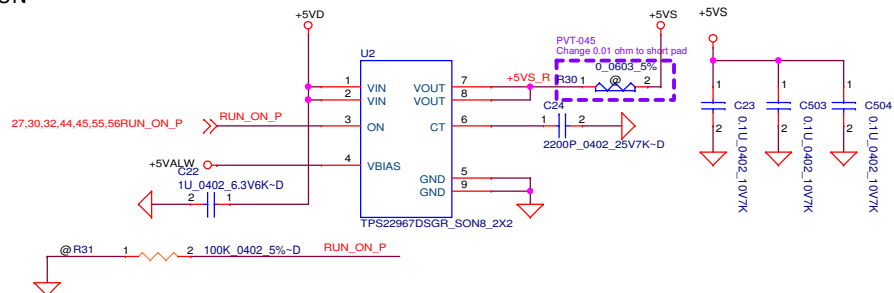
UART BIOS debug

ESPI BIOS debug

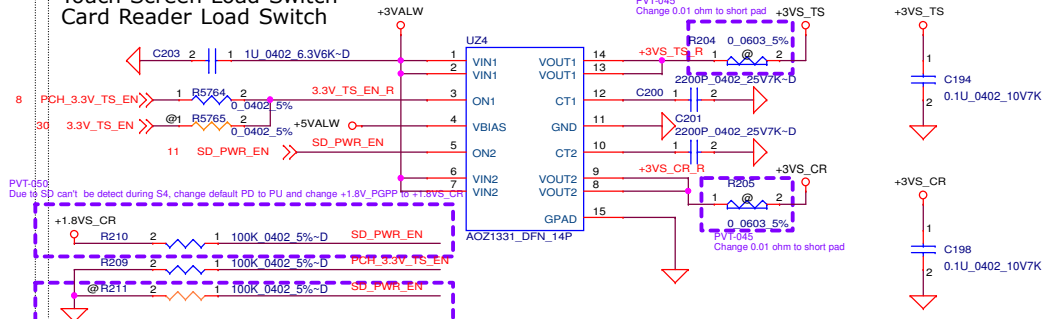
IR CAM CONN



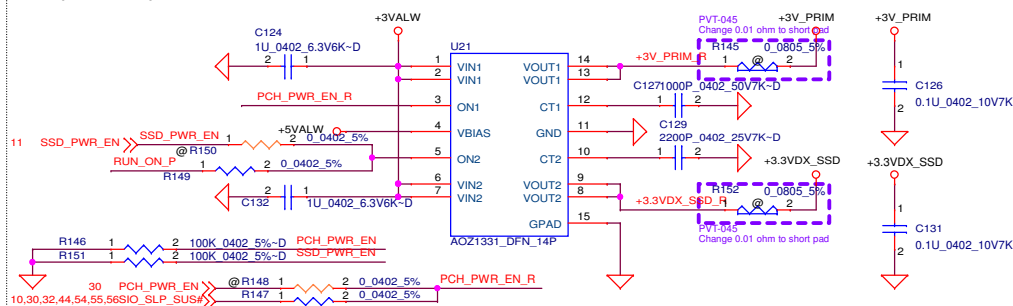
+5V RUN



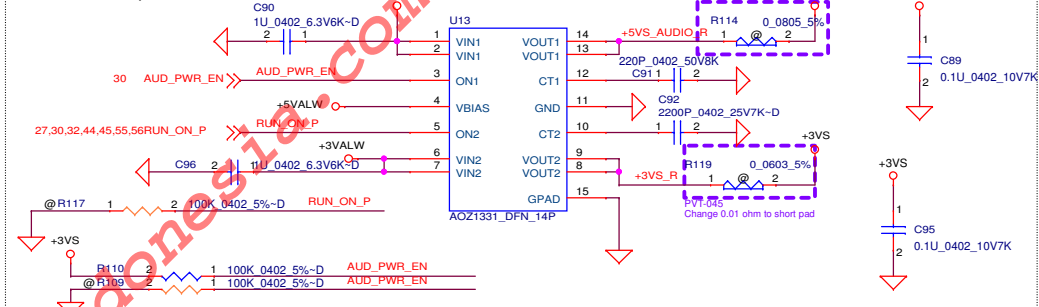
Touch Screen Load Switch Card Reader Load Switch



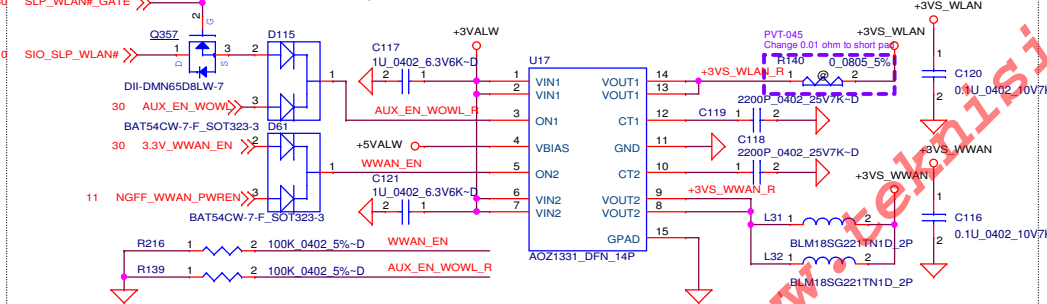
Deeper Sleep, SSD Load Switch



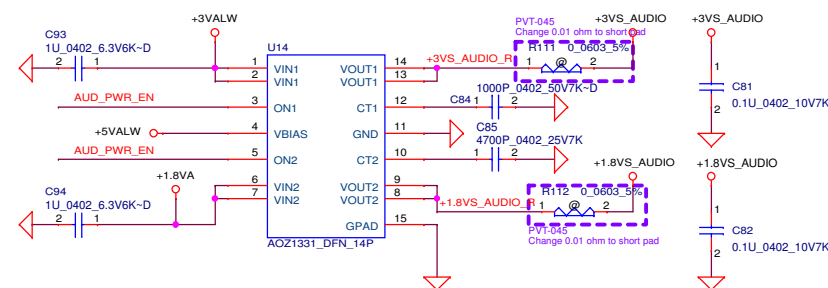
+5V Audio , 3V Run



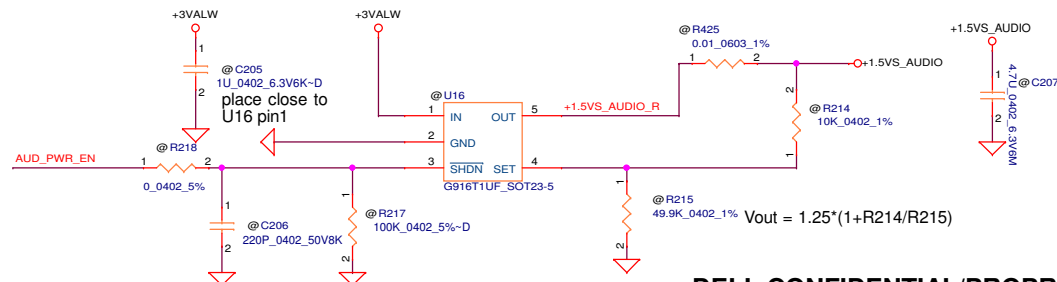
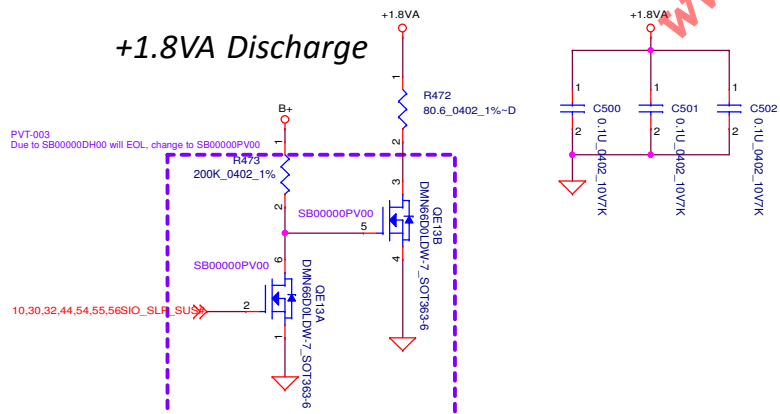
WLAN/WWAN Load Switch



3V Audio, 1.8V_Audio Load Switch



+1.8VA Discharge

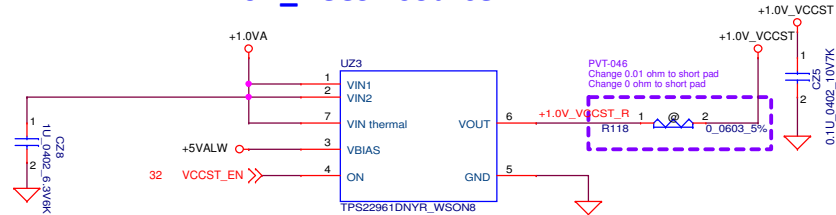


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						P44-DC/DC Interface 1	
						Size	Document Number
						LA-F371P	
						Date:	Tuesday, November 07, 2017
						Sheet	44 of 65

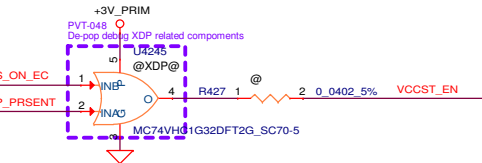
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.

LA-F371P
Rev 1.0

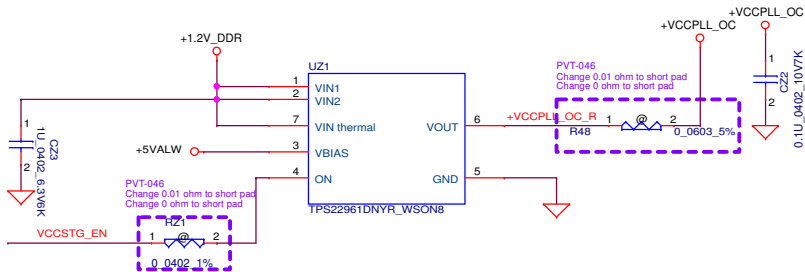
+1.0V_VCCST source



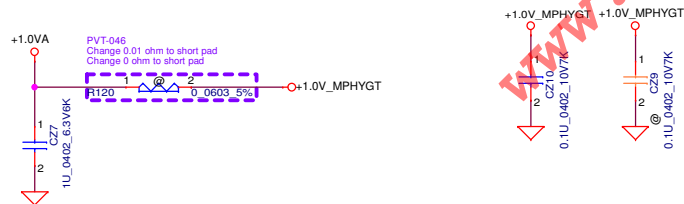
BEAVER CREEK:
4.4mohm/6A
TR=12.5us@Vin=1.05V



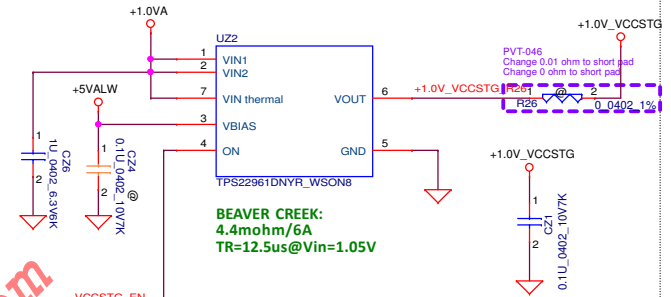
+VCCPLL_OC source



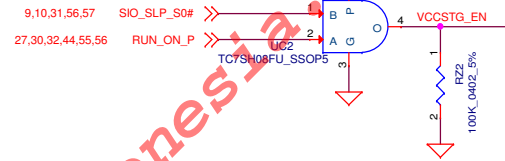
+1.0V_MPHYGT source



+1.0V_VCCSTG source

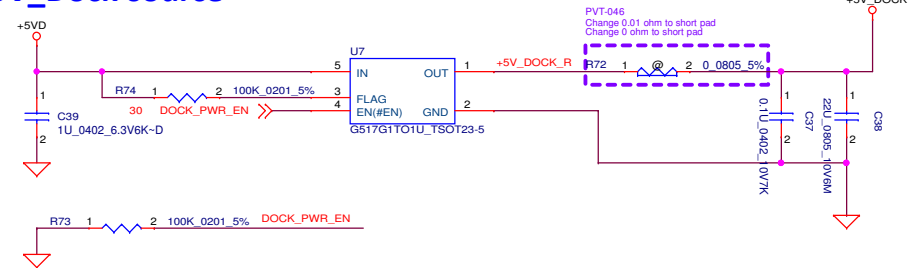


BEAVER CREEK:
4.4mohm/6A
TR=12.5us@Vin=1.05V

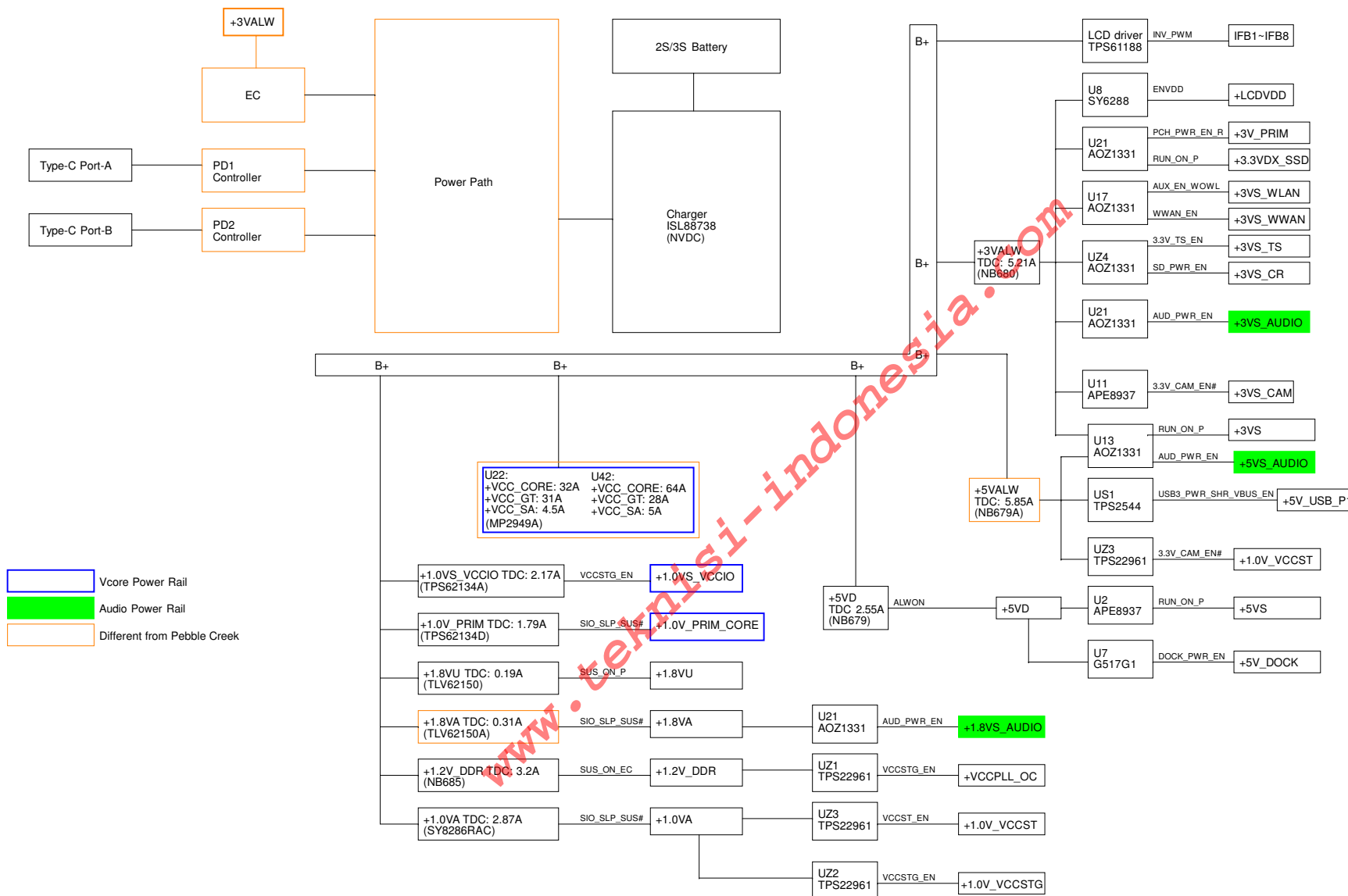


	S0	S0Ix	S3
SIO_SLP_S0#	high	low	low
RUN_ON_EC	high	high	low

+5V_Dock source

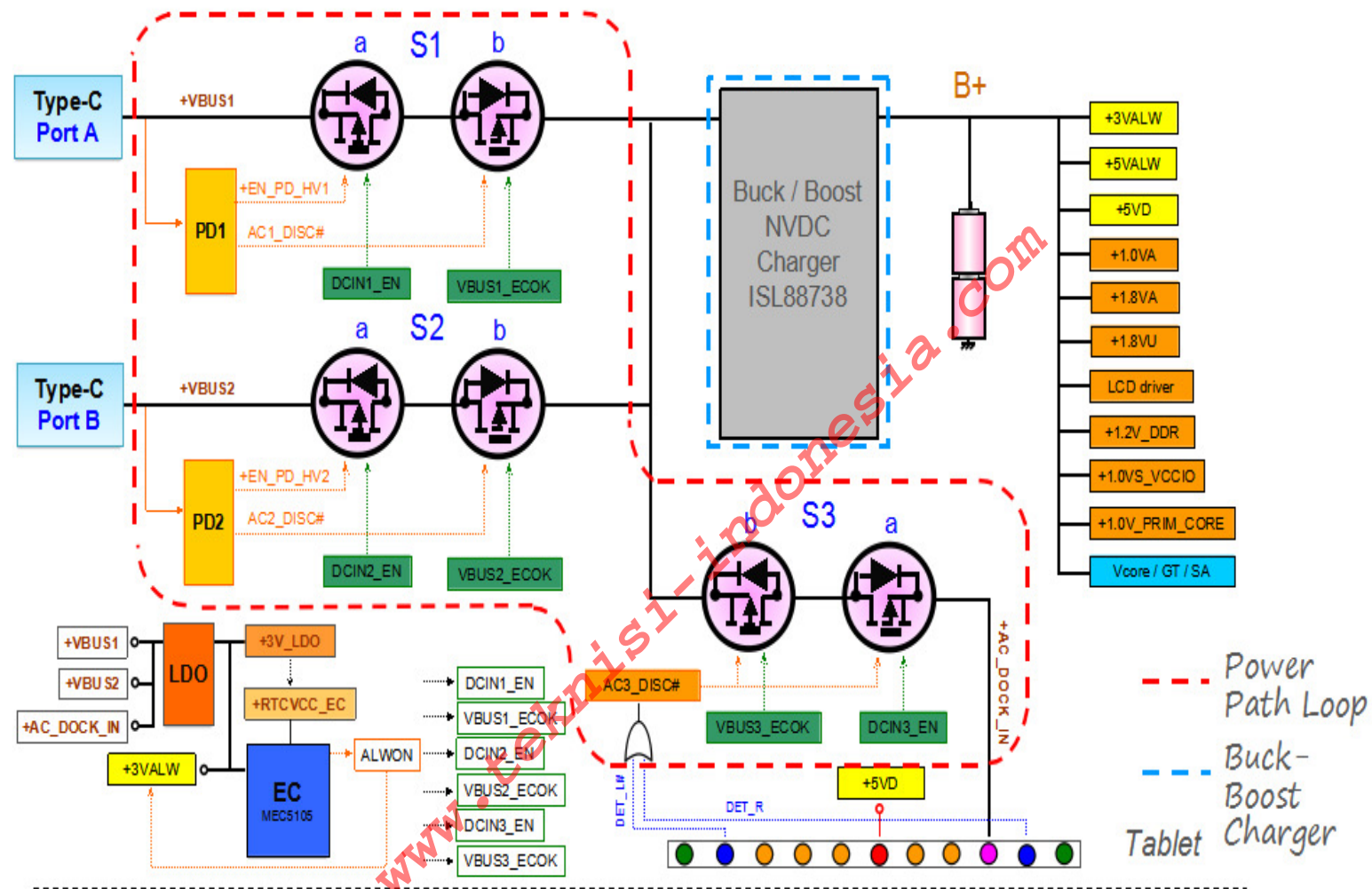


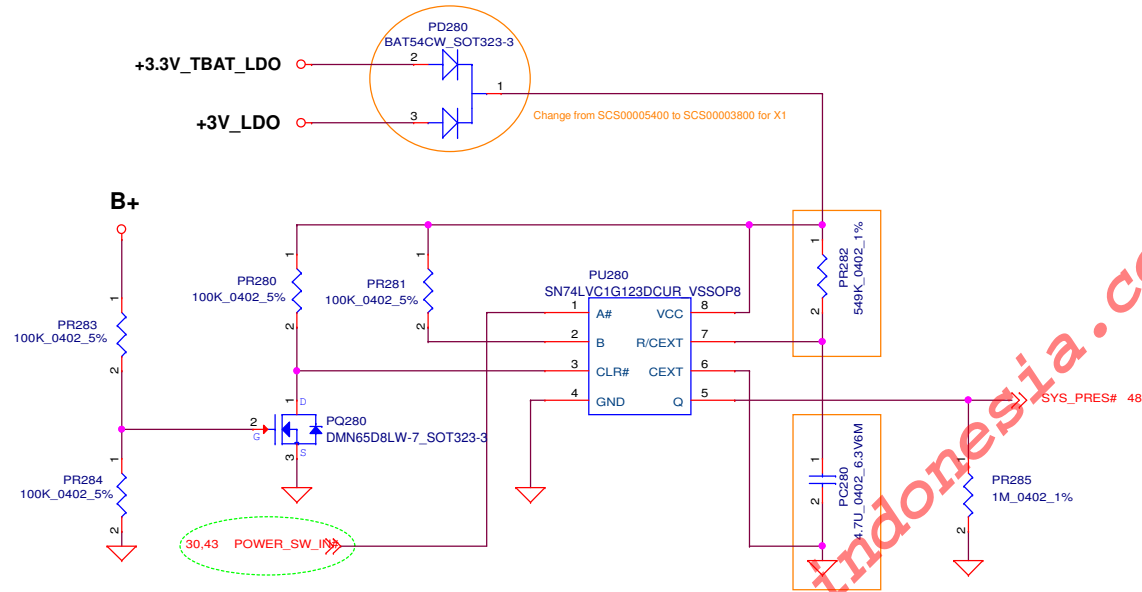
Pebble Creek MLK Power Block - Tablet



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				PWR POWER BLOCK DIAGRAM	
				Size	Document Number
				Rev	1.0
				Page	1 of 1

Pebble Creek MLK Power Path Block

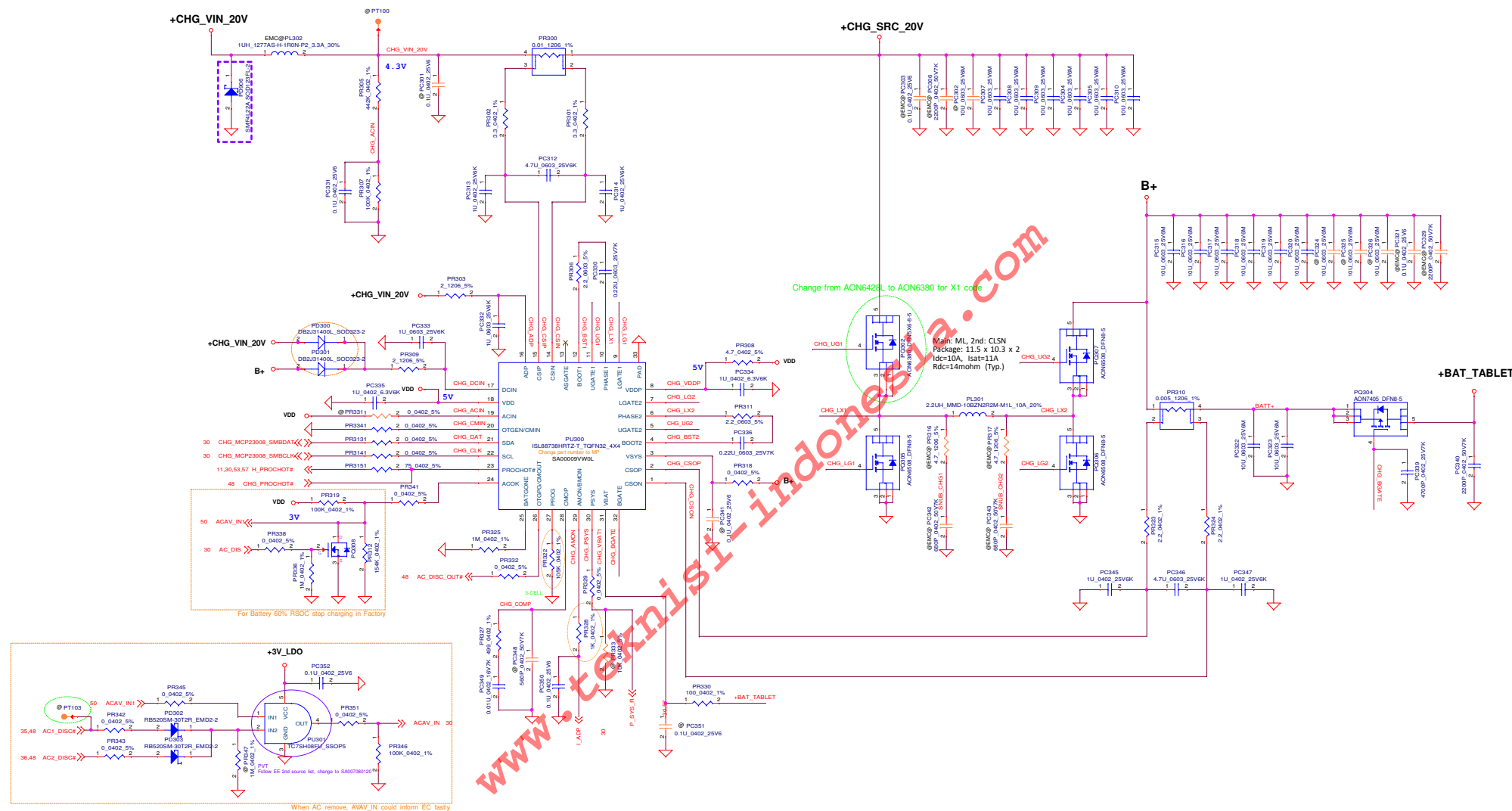




FUNCTION TABLE

INPUTS			OUTPUTS
CLR	A	B	Q
L	X	X	L
X	H	X	L ⁽¹⁾
X	X	L	L ⁽¹⁾
H	L	↑	⌋
H	↓	H	⌋
↑	L	H	⌋

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				Size	Document Number
				Date:	Tuesday, November 07, 2017
				Sheet	49 of 65
				Rev	1.0



Change from AON6428L to AON6380 for X1 code

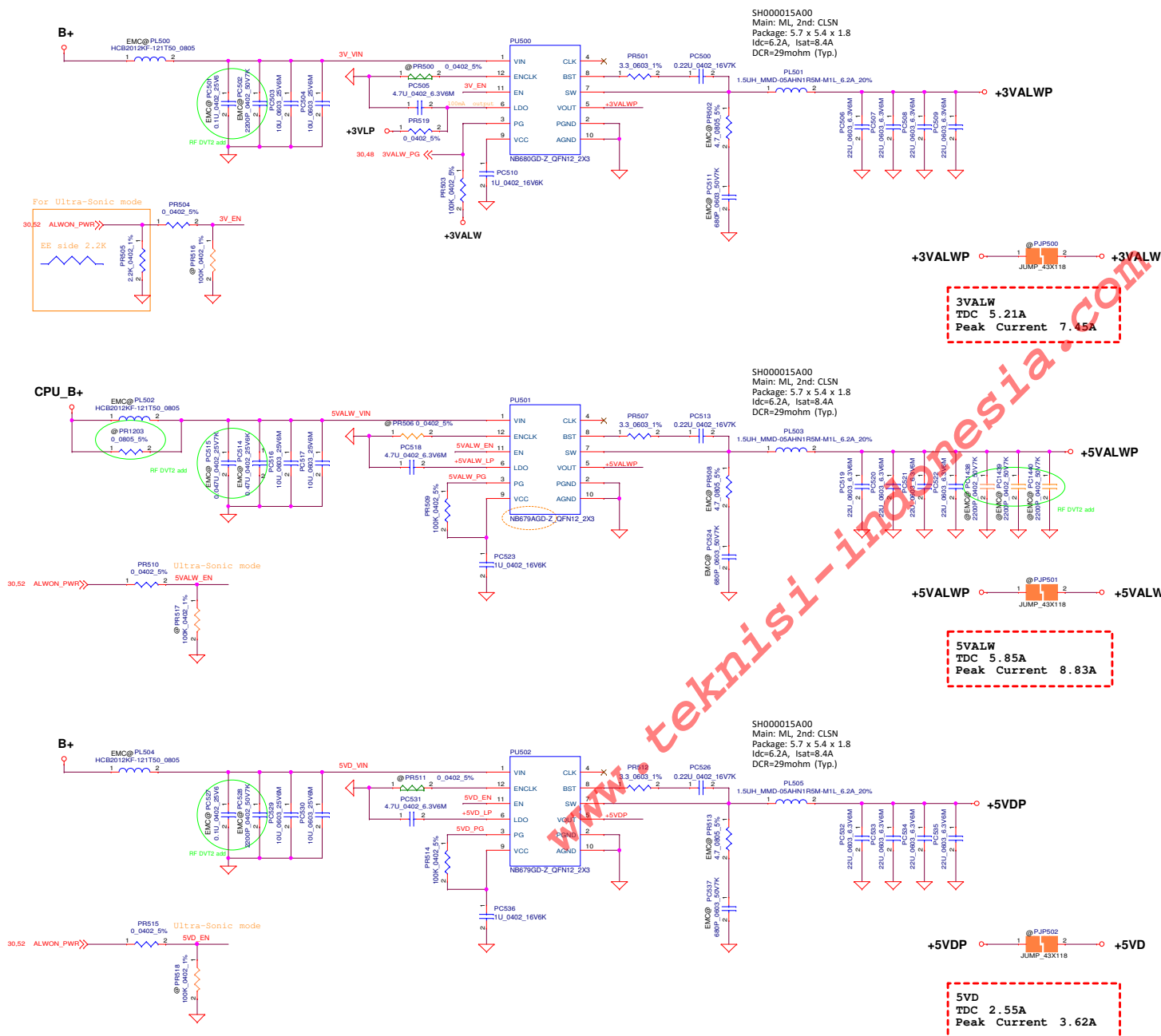
Main: ML, 2nd: CLSN
Package: 11.5 x 10.3 x 2
Idc=10A, Isat=11A
Rdc=14mohm (Typ.)

For Battery 60% RSOC stop charging in Factory

When AC remove, ACAV_IN could inform 'EC' fastly

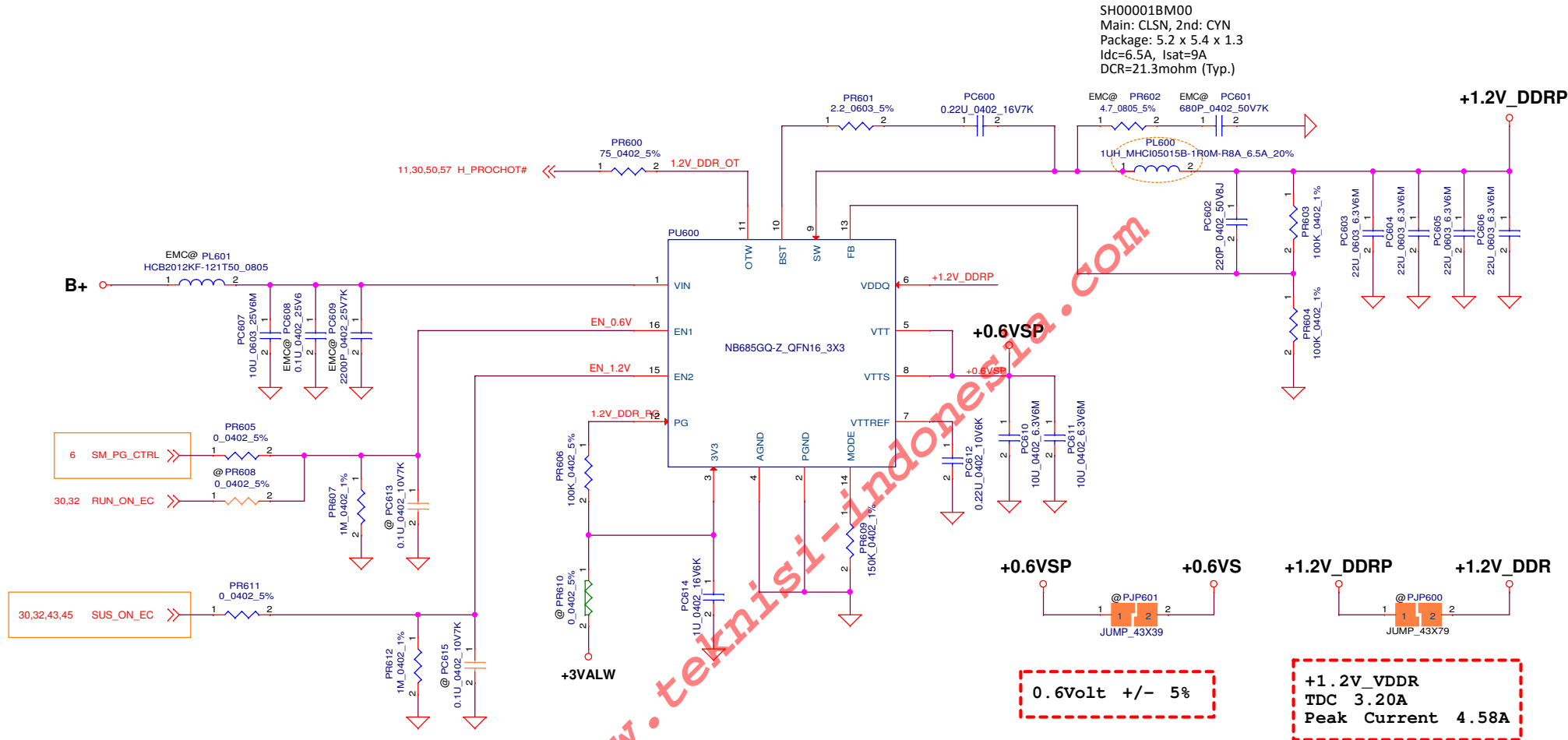
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/10/24	Deciphered Date	2015/08/31	Title	PWR Charger (ISL88738)
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Size	Document	Number			1.0
Date	Tuesday, November 07, 2017	Sheet	50	of	65

3V/5V controller(35.1), Support component(35.2)



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Issued Date	2011/06/02	Deciphered Date	2013/10/28	PWR +3V(NB680)/+5V(NB679) LA-F371P	
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MAY BE REDUCED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Drawing Number: 017, 017 Date: Tuesday, November 07, 2017	Sheet: 52 of 66 Rev: 1.0

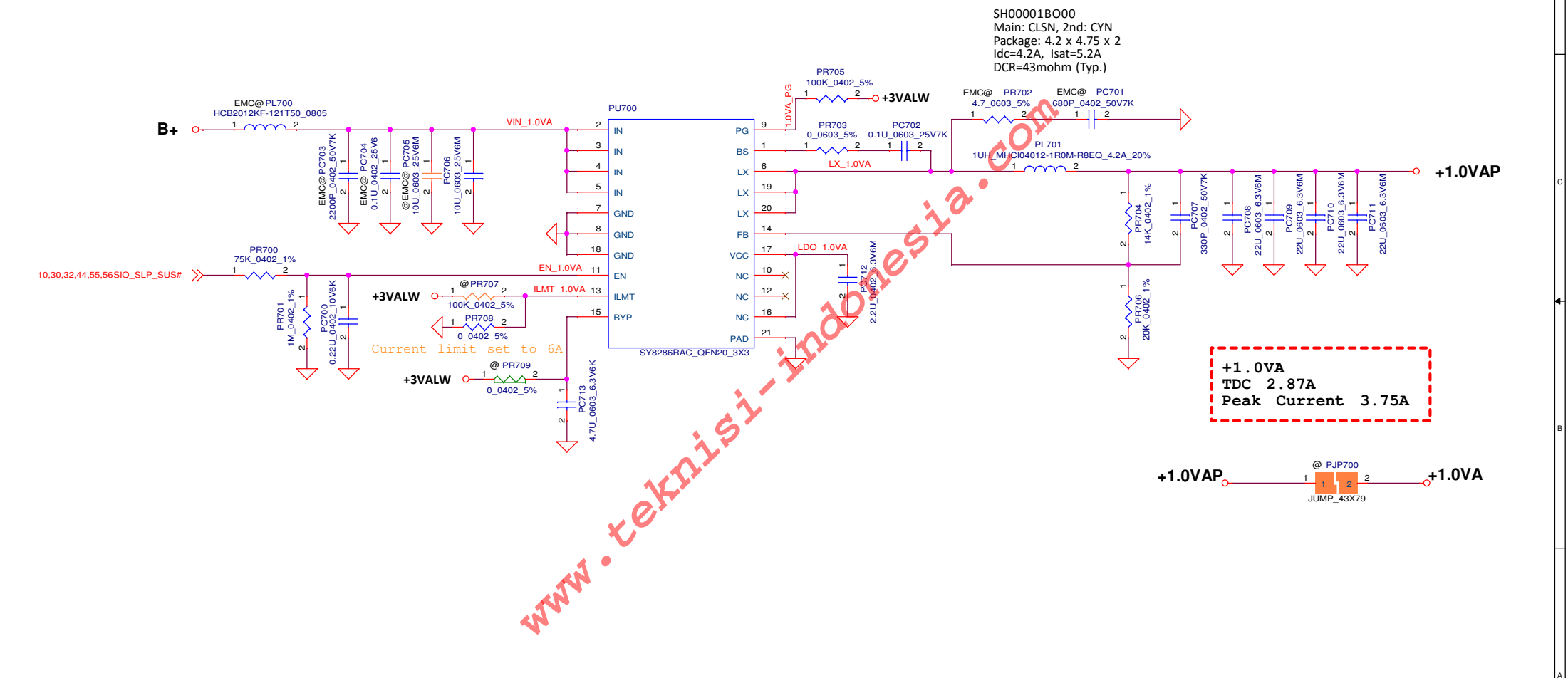
+1.2V_DDR controller(35.3), Support component(35.4)



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				Size	Document Number
				Date:	Tuesday, November 07, 2017
				Sheet	53 of 65
				Rev	1.0

Module Design

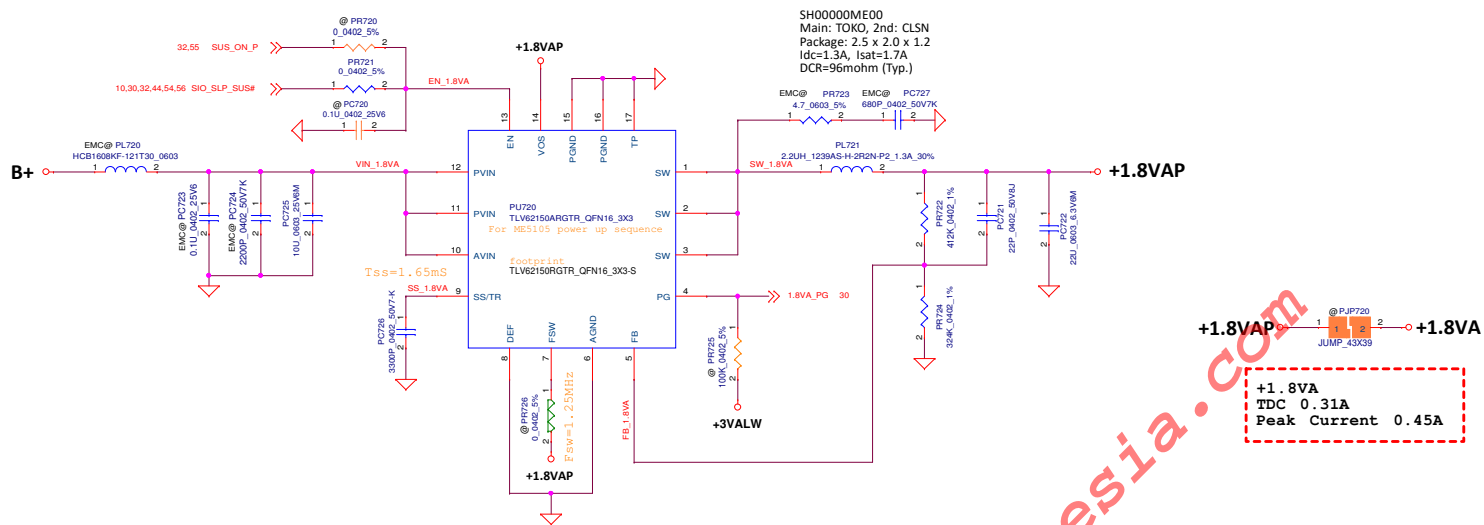
+1.0VA controller(35.5), Support component(35.6)



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Date: Tuesday, November 07, 2017		Sheet 54 of 65		Size	Document Number
				LA-F371P	Rev 1.0

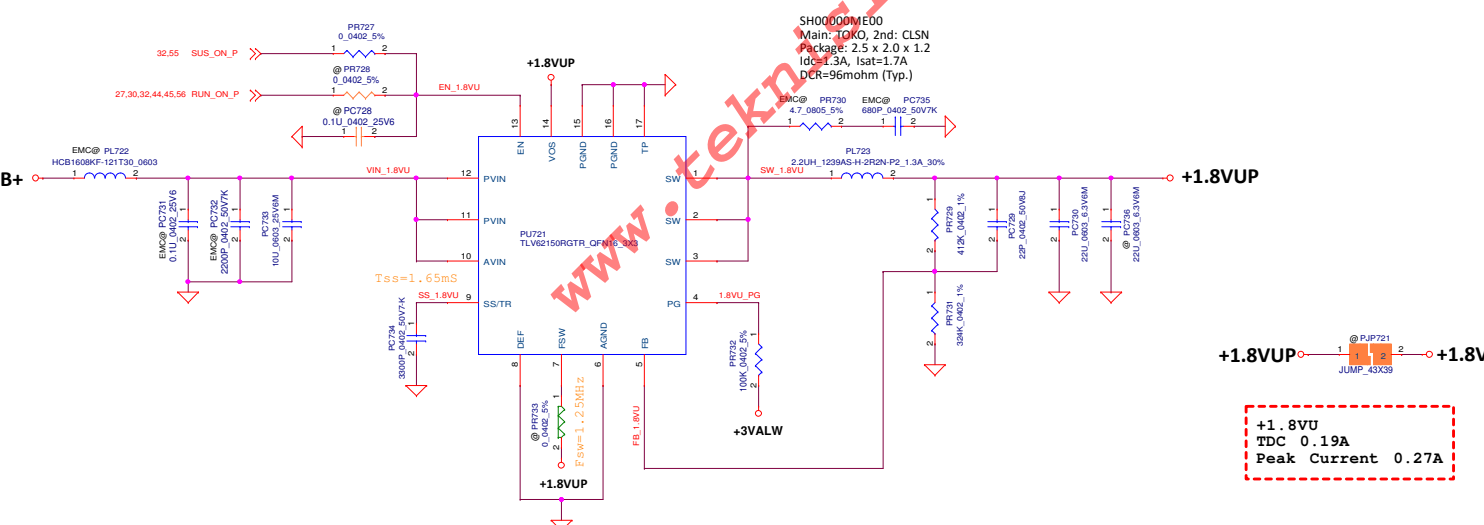
Module Design

+1.8VS controller(35.13), Support component(35.14)

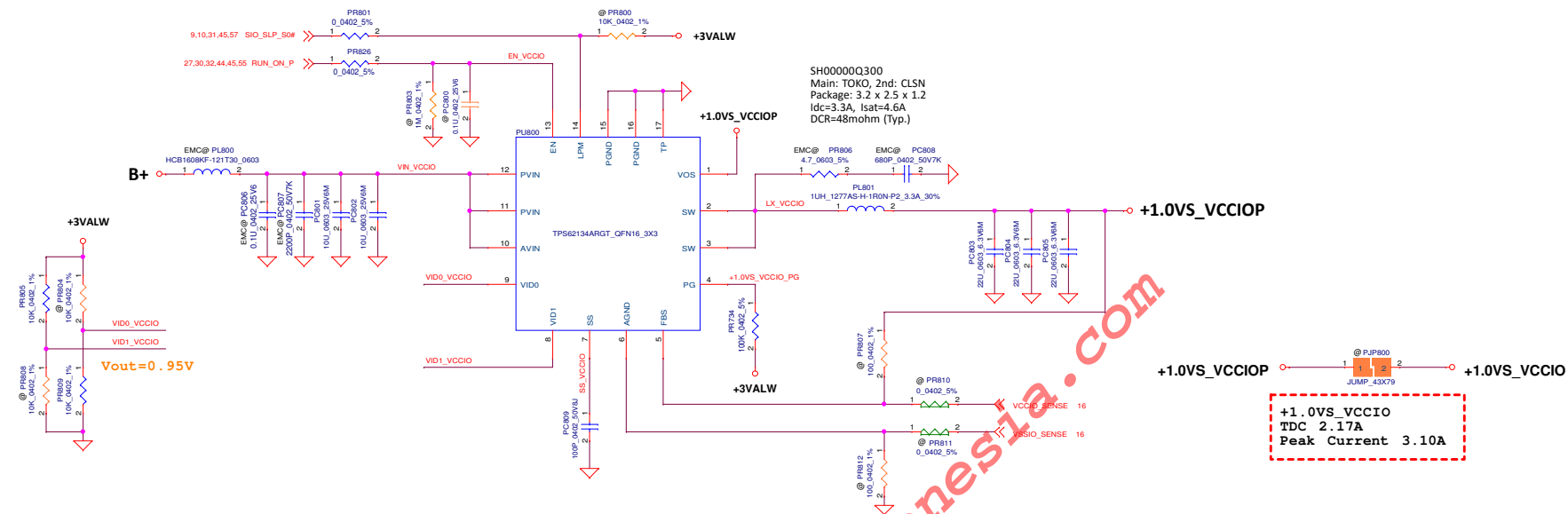


Module Design

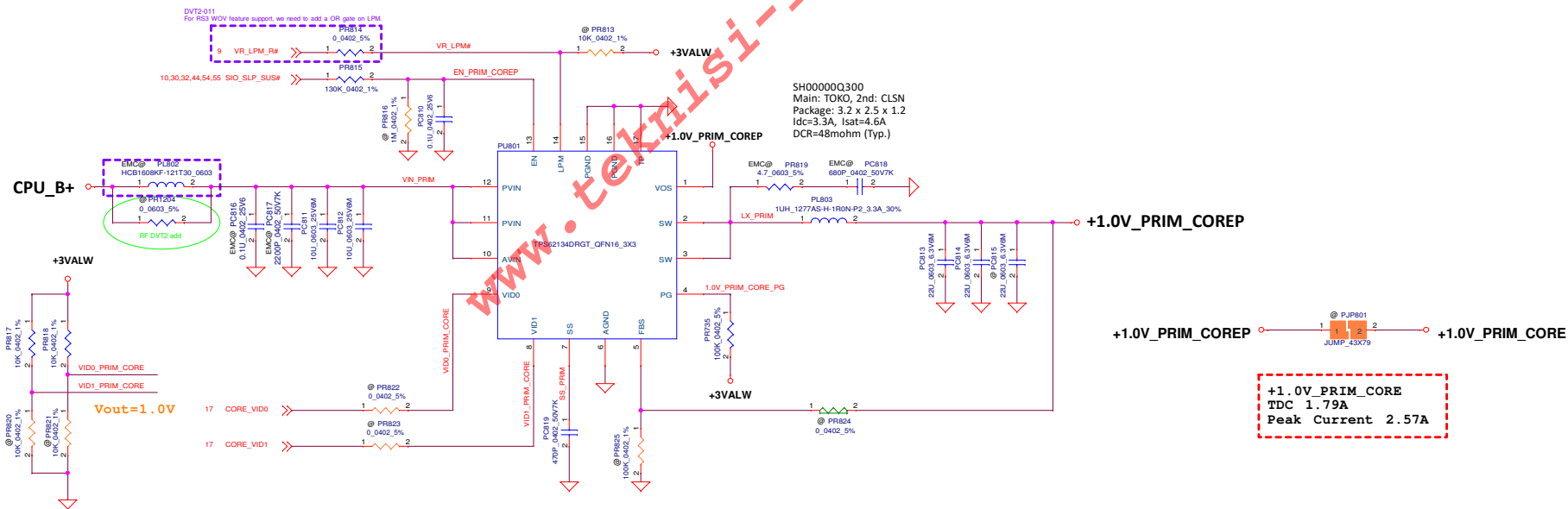
+1.8VU controller(35.15), Support component(35.16)



+1.0VS_VCCIO controller(35.11), Support component(35.12)

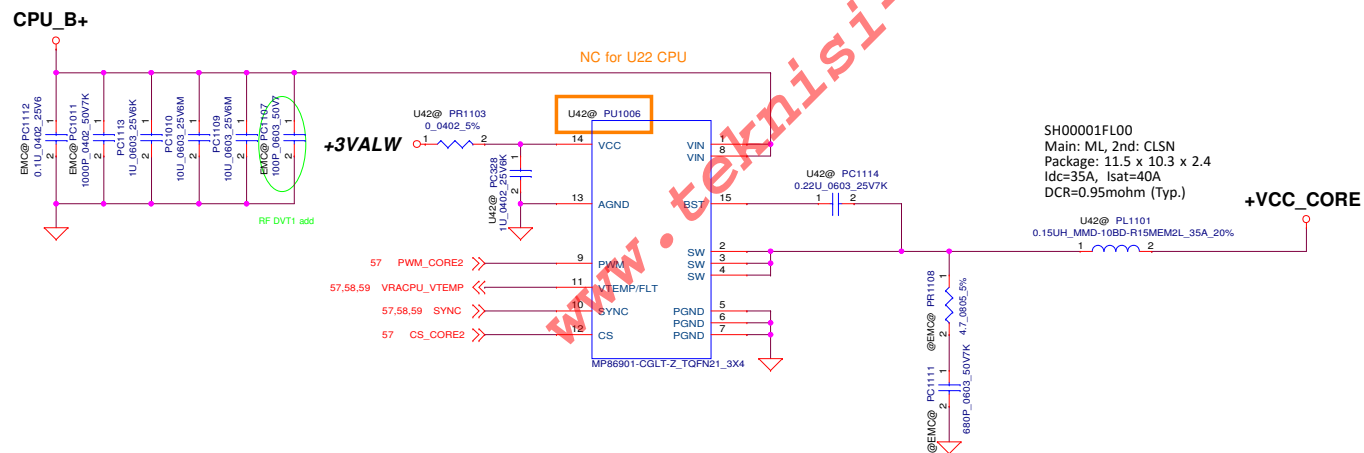
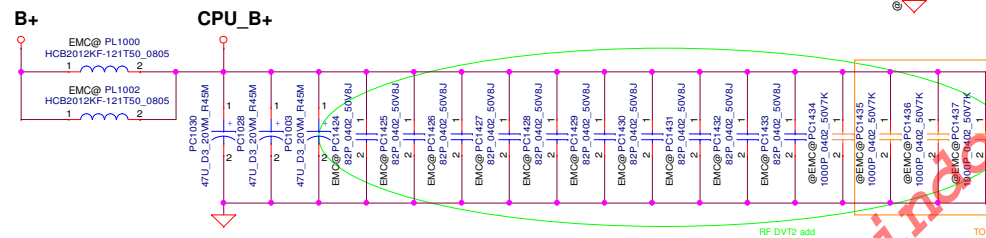
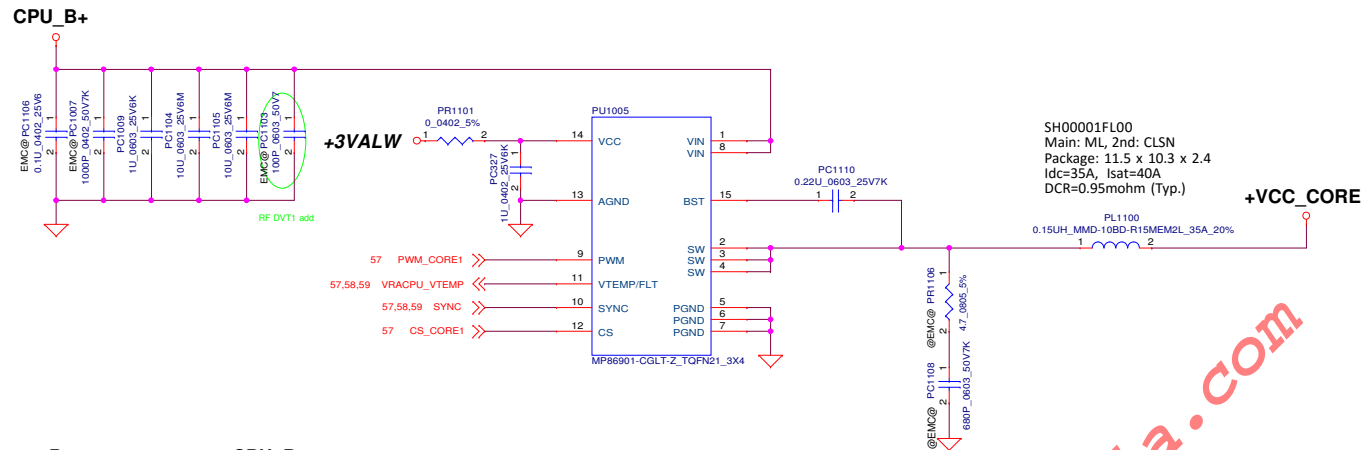


+1.0V_PRIM_CORE controller(35.7), Support component(35.8)



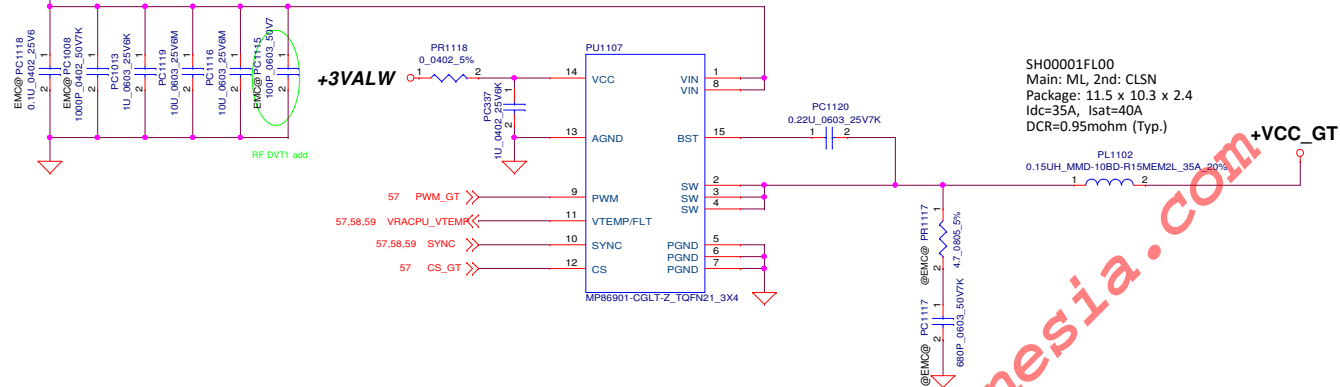
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Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title	PWR_VCCIO/PRIM(TPS62134*2)	
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				LA-F371P		1.0
				Date:	Tuesday, November 07, 2017	Sheet

VCC_CORE Dr. MOS (36.2), Support component(36.3)

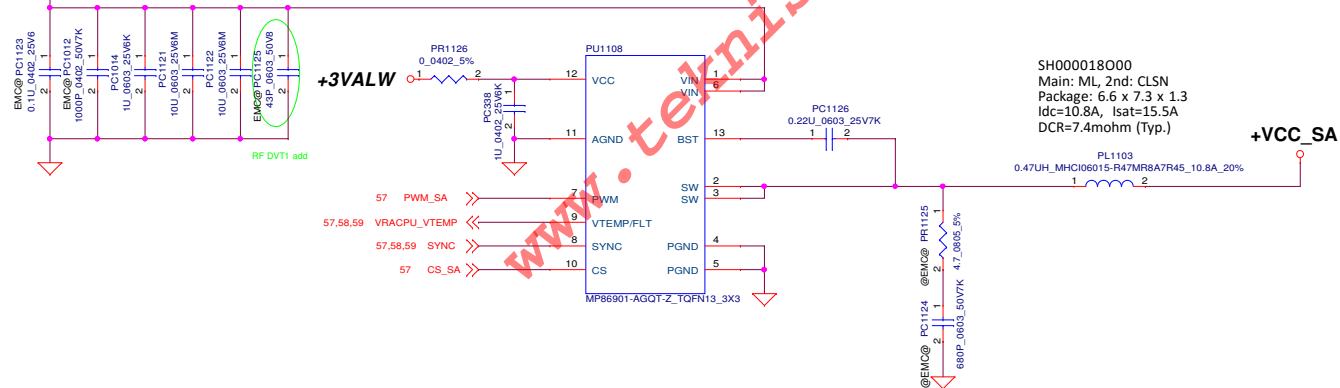


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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title PWR_+VCORE		
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				LA-F371P		
				Date:	Tuesday, November 07, 2017	Sheet 58 of 65

CPU_B+



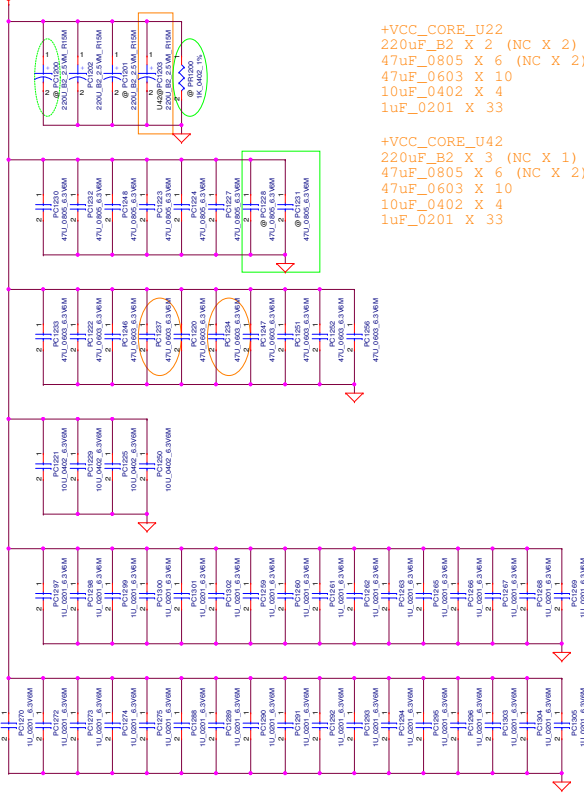
CPU_B+



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					LA-F371P	1.0
				Date:	Tuesday, November 07, 2017	Sheet 59 of 65

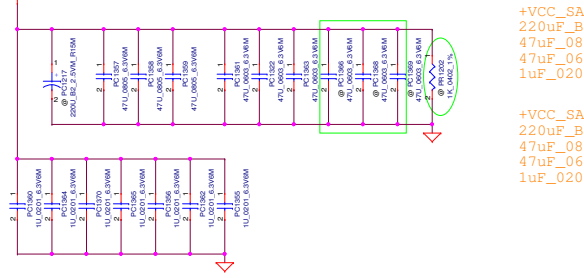
VCC_CORE output cap(36.4), VCC_GT output cap(36.5), VCC_SA output cap(36.6), VCCIA_GT output cap(36.7)

+VCC_CORE



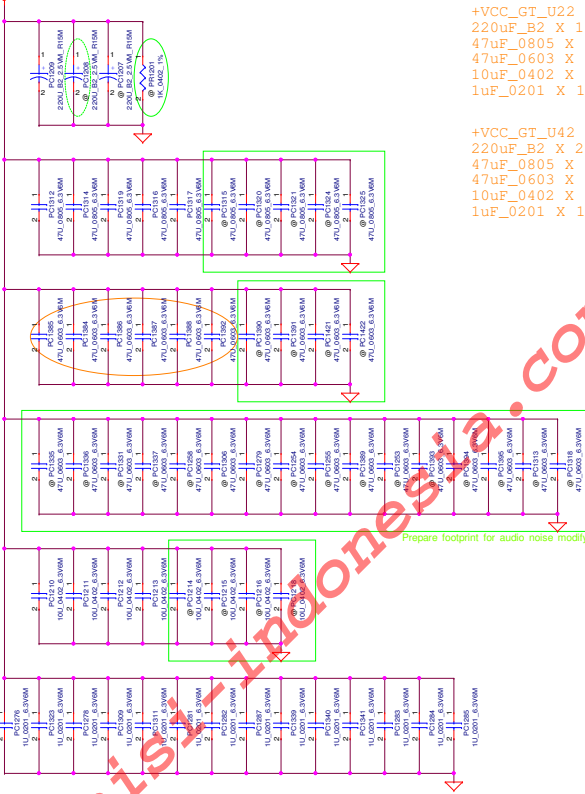
- +VCC_CORE_U22
220uF_B2 X 2 (NC X 2)
47uF_0805 X 6 (NC X 2)
47uF_0603 X 10
10uF_0402 X 4
1uF_0201 X 33
- +VCC_CORE_U42
220uF_B2 X 3 (NC X 1)
47uF_0805 X 6 (NC X 2)
47uF_0603 X 10
10uF_0402 X 4
1uF_0201 X 33

+VCC_SA



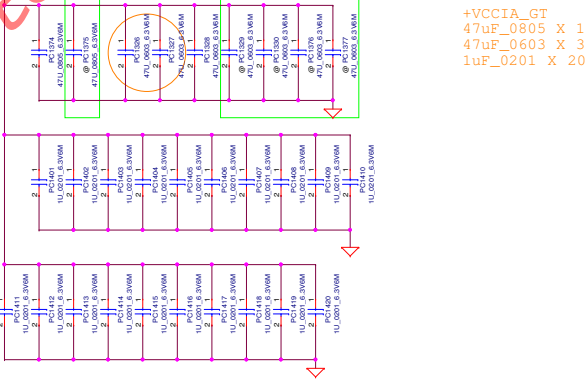
- +VCC_SA_U22
220uF_B2 X 0 (NC X 1)
47uF_0805 X 3
47uF_0603 X 3 (NC X 3)
1uF_0201 X 7
- +VCC_SA_U42
220uF_B2 X 0 (NC X 1)
47uF_0805 X 3
47uF_0603 X 3 (NC X 3)
1uF_0201 X 7

+VCC_GT

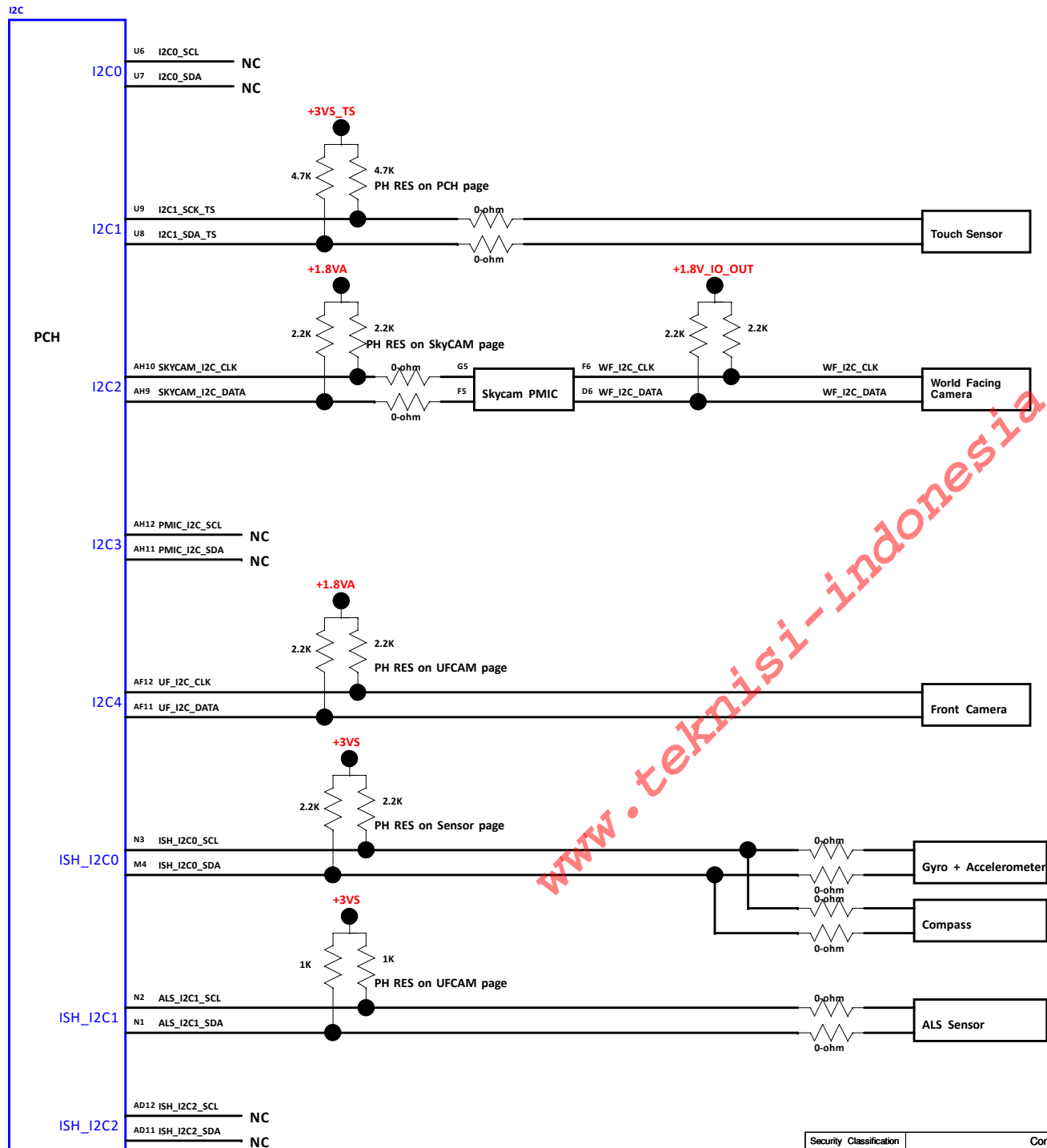


- +VCC_GT_U22
220uF_B2 X 1 (NC X 2)
47uF_0805 X 5 (NC X 5)
47uF_0603 X 6 (NC X 20)
10uF_0402 X 4 (NC X 4)
1uF_0201 X 14
- +VCC_GT_U42
220uF_B2 X 2 (NC X 1)
47uF_0805 X 5 (NC X 5)
47uF_0603 X 6 (NC X 20)
10uF_0402 X 4 (NC X 4)
1uF_0201 X 14

+VCCIA_GT

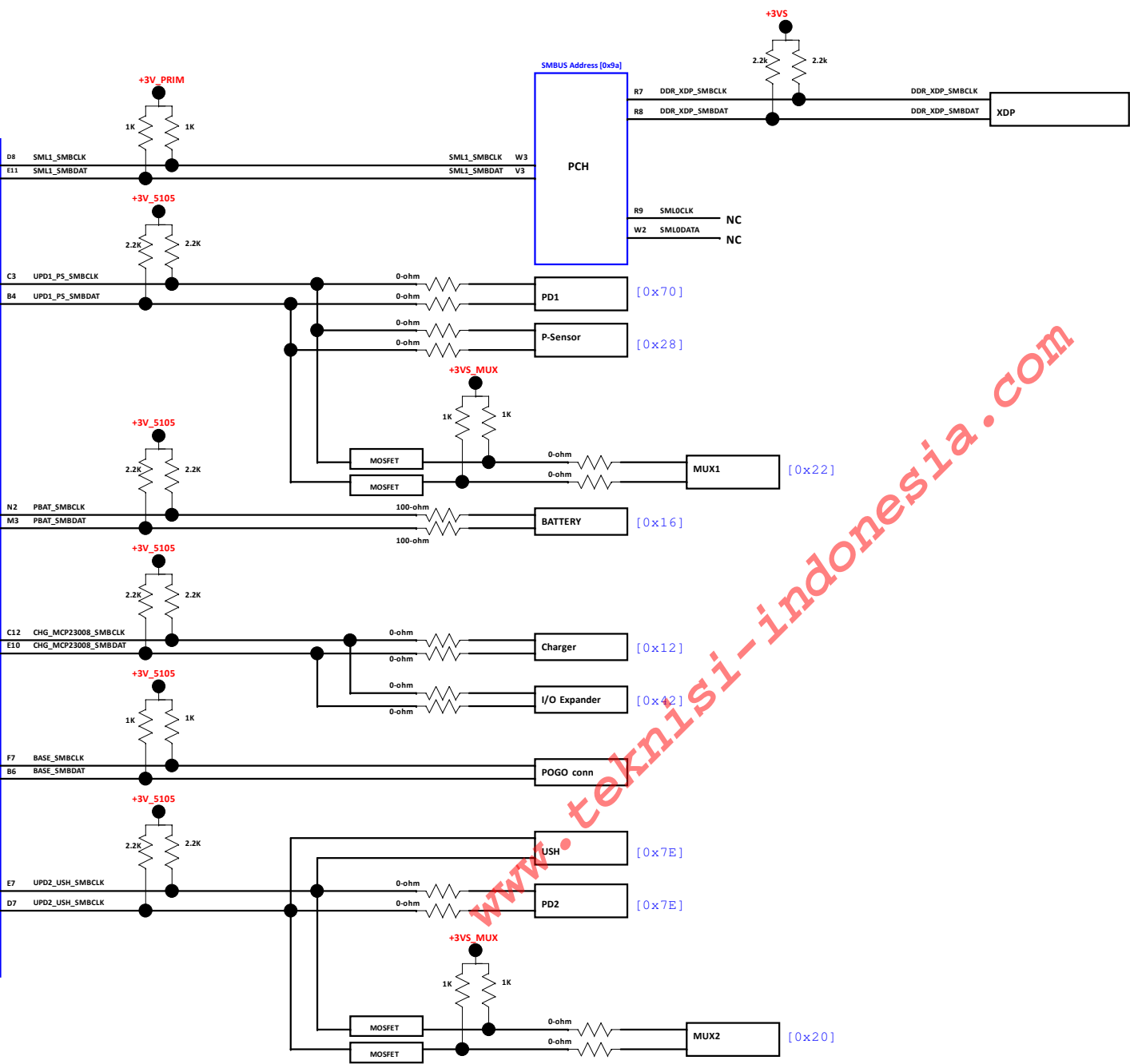


- +VCCIA_GT
47uF_0805 X 1 (NC X 1)
47uF_0603 X 3 (NC X 4)
1uF_0201 X 20



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Size	Document Number			Rev	1.0
Date:	Tuesday, November 07, 2017	Sheet	61	of	65

HEAD EC
5105



Discrete Power On Sequence

[AC in]

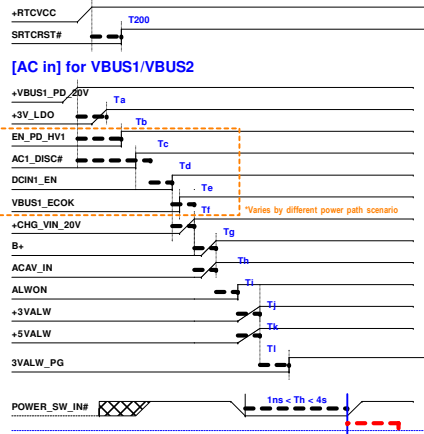
[Battery only, AC absent]

ITEM	Measure Point	Time
Ta	+VBUS_PD_20V	To
Tb	3V_LDO	To
Tc	EN_PD_HV1	To
Td	EN_PD_HV1	To
Te	ACT_DISC#	To
Tf	DCIN1_EN	To
Tg	VBUS1_ECOK	To
Th	+CHG_VIN_20V	To
Ti	B+	To
Tj	ACAV_IN	To
Tk	ALWON	To
Tl	+3VALW	To
Tm	+5VALW	To
Tn	3VALW_PG	To

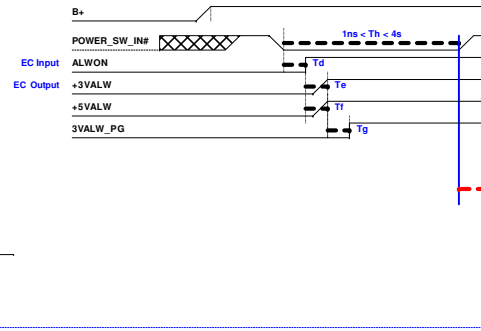
ITEM	Measure Point	Time
Ta	+VBUS_PD_20V	To
Tb	3V_LDO	To
Tc	EN_PD_HV1	To
Td	EN_PD_HV1	To
Te	ACT_DISC#	To
Tf	DCIN1_EN	To
Tg	VBUS1_ECOK	To
Th	+CHG_VIN_20V	To
Ti	B+	To
Tj	ACAV_IN	To
Tk	ALWON	To
Tl	+3VALW	To
Tm	+5VALW	To
Tn	3VALW_PG	To

ITEM	Measure Point	Time
T1	DSW_ON	To
T2	+3VALW_DSW	To
T3	+3VALW_DSW	To
T4	PCH_DPWRK	To
T5	SIO_SLP_SUS#	To
T6	PCH_DPWRK	To
T7	SIO_SLP_SUS#	To
T8	PCH_PWR_EN	To
T9	PCH_PWR_EN	To
T10	PCH_PWR_EN	To
T11	PCH_PWR_EN	To
T12	PCH_PWR_EN	To
T13	PCH_PWR_EN	To
T14	PCH_PWR_EN	To
T15	PCH_PWR_EN	To
T16	PCH_PWR_EN	To
T17	PCH_PWR_EN	To
T18	PCH_PWR_EN	To
T19	PCH_PWR_EN	To
T20	PCH_PWR_EN	To
T21	PCH_PWR_EN	To
T22	PCH_PWR_EN	To
T23	PCH_PWR_EN	To
T24	PCH_PWR_EN	To
T25	PCH_PWR_EN	To
T26	PCH_PWR_EN	To
T27	PCH_PWR_EN	To
T28	PCH_PWR_EN	To
T29	PCH_PWR_EN	To
T30	PCH_PWR_EN	To
T31	PCH_PWR_EN	To
T32	PCH_PWR_EN	To
T33	PCH_PWR_EN	To
T34	PCH_PWR_EN	To
T35	PCH_PWR_EN	To
T36	PCH_PWR_EN	To
T37	PCH_PWR_EN	To
T38	PCH_PWR_EN	To
T39	PCH_PWR_EN	To
T40	PCH_PWR_EN	To
T41	PCH_PWR_EN	To
T42	PCH_PWR_EN	To

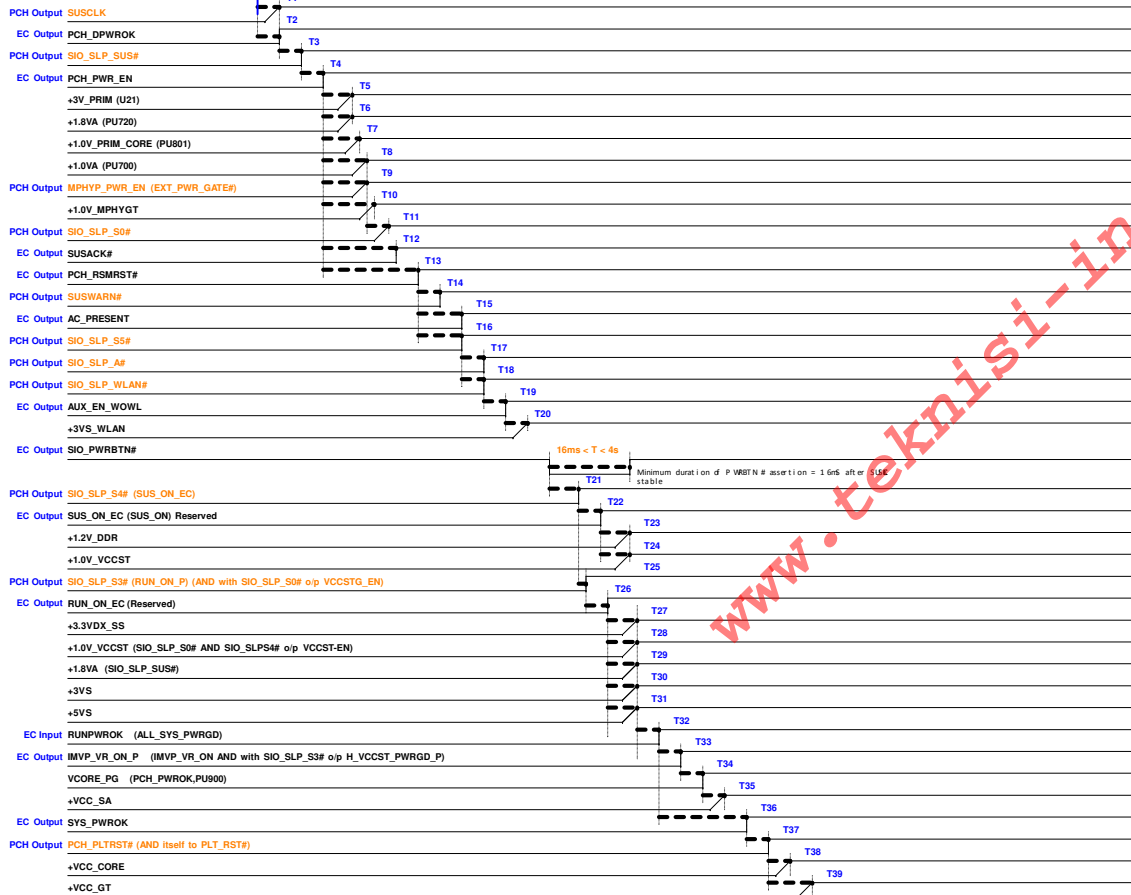
update



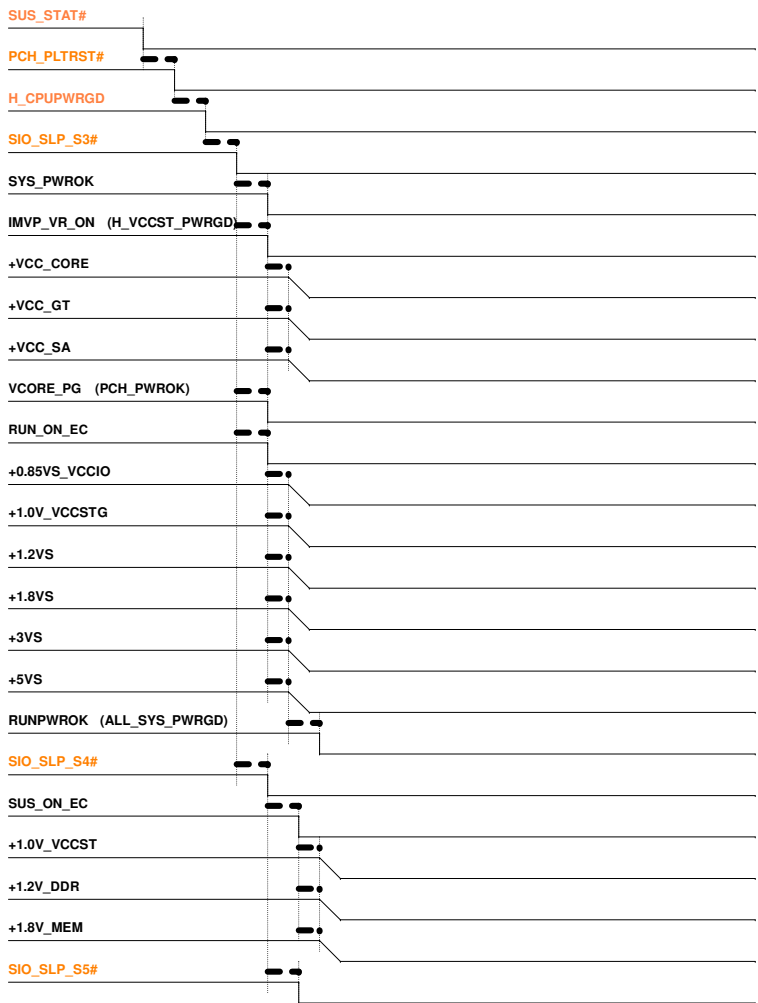
[Battery only, AC absent]



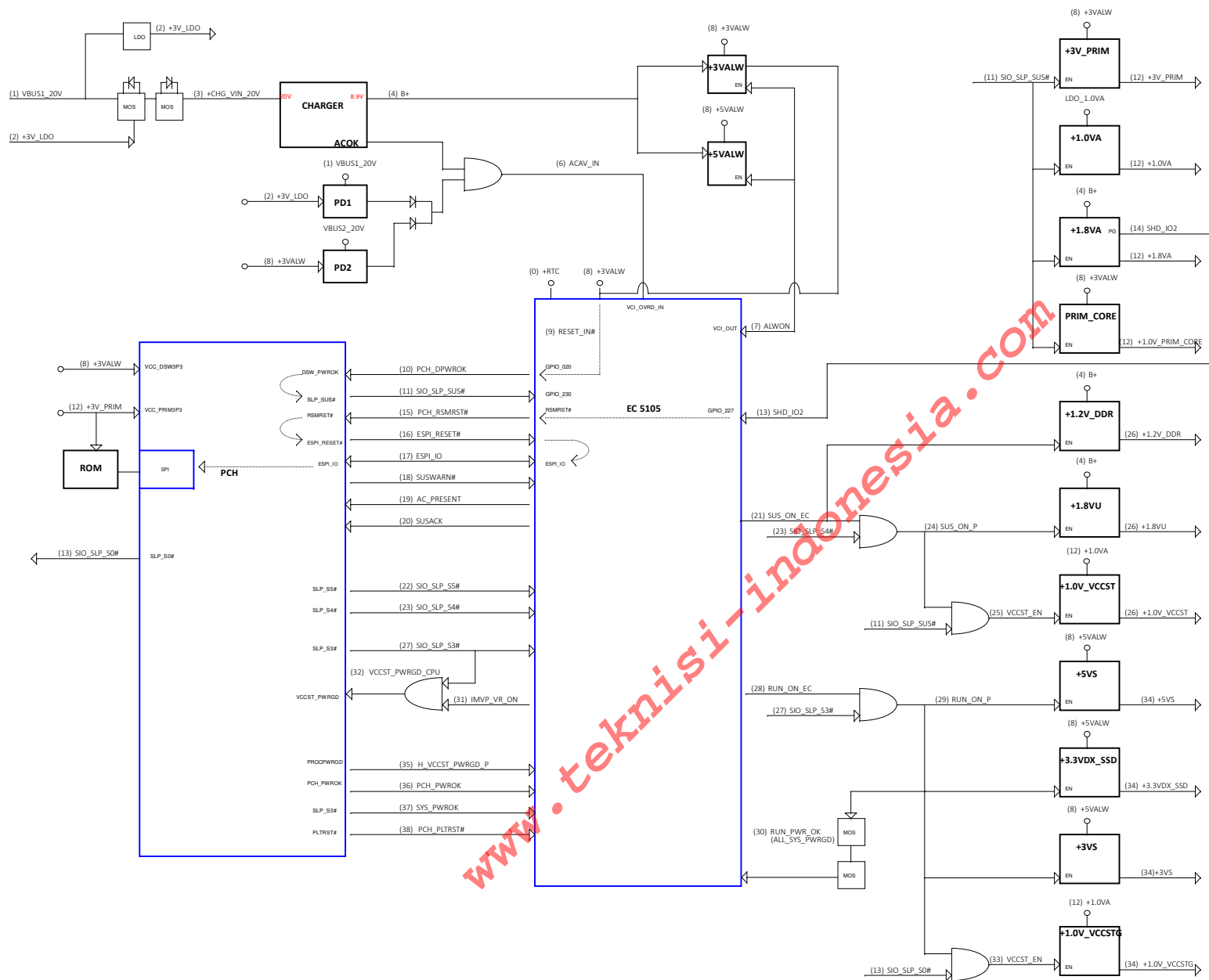
EC pay attention timing



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Size		Document Number			Rev
Date: Tuesday, November 07, 2017		Sheet 64 of 65			1.0



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REV				Size	Document Number
1.0				1/1	1/1